International Journal of the Physical Sciences Vol. 6(32), pp. 7341 - 7353, 2 December, 2011
Available online at http://www.academicjournals.org/IJPS
DOI: 10.5897/IJPS11.1202
ISSN 1992 - 1950 ©2011 Academic Journals

Full Length Research Paper

Leakage power reduction techniques of 45 nm static random access memory (SRAM) cells

Manish Dev Singh[1]*, Shyam Akashe[2] and Sanjay Sharma[2]

[1]Department of Electronics and Communication Engineering, RGPV University, Bhopal, M. P., India.
[2]Department of Electronics and Communication Engineering, Thapar University, Patiala, Punjab, India.

Accepted 23 August, 2011

As the technology scales down to 90 nm and below, static random access memory (SRAM) standby leakage power is becoming one of the most critical concerns for low power applications. In this article, we review three major leakage current components of SRAM cells and also discuss some of the leakage current reduction techniques including body biasing, source biasing, dynamic V_{DD}, negative word line, and bit line floating schemes. All of them are achieved by controlling different terminal voltages of the SRAM cell in standby mode. On the other hand, performance loss occurs simultaneously with leakage saving. To validate the effectiveness of low power techniques, the leakage current, static noise margin, and read current of SRAM cells, based on the UMC 45 nm complementary metal–oxide–semiconductor (CMOS) process with leakage current reduction techniques has been simulated. The results indicate that by using the dynamic V_{DD} and source biasing schemes, greater leakage suppressing capability, although with a higher performance loss, can be obtained. Therefore, the SRAM cell optimization scheme must consider the trade-off between power consumption and speed performance.

Key words: Bit line floating, body biasing, Dynamic VDD, low power design, negative word line, source biasing, static random access memory (SRAM).

INTRODUCTION

The area and power consumption of the SOC devices, occupied by static random access memory (SRAM), increase largely with technology scaling. Thus they are critical components in both high-performance processors and hand-held applications. As a result, SRAM energy power becomes a major issue, and low power SRAM designs, without compromising speed performance, are especially crucial in modern very-large-scale integration (VLSI) designs. In fact, considerable attention has been contributed to the reduction of leakage current from SRAM cells, in order to improve the system's power efficiency, performance, reliability and overall costs. The SRAM cell consumes energy in both dynamic and static ways. Historically, the primary source of power dissipation has been dynamic energy due to word line decoding, bit line charging/discharging, sense amplification, output driving, and so on. As we move into sub-micron technology, scaling of the transistor threshold voltage sharply increases the sub threshold leakage current, whereas, the ultra-thin gate oxide results in an exponential increase in gate leakage current. Figure 1 show the SRAM leakage current with technology scaling and it indicates that the leakage current has dramatically increased when technology scales down to 90 nm and below. Therefore, many solutions devoted to solve this problem have been presented (Razavipour et al., 2009; Heo et al., 2002). In this article, we review some of the leakage current reduction techniques in the circuit level of a 7T-SRAM cell and make some related simulations and analyses based on the UMC 45 nm complementary metal–oxide–semiconductor (CMOS) process.

LEAKAGE CURRENT COMPONENTS

There are several major sources of leakage current, that is, the sub threshold current due to low threshold voltage, the gate leakage current due to very thin gate oxides, and the band-to-band tunneling current due to the heavily doped

*Corresponding author. E-mail: ma4nish@gmail.com. Tel: +91-9425146040. Fax: +91-0751-2432988.

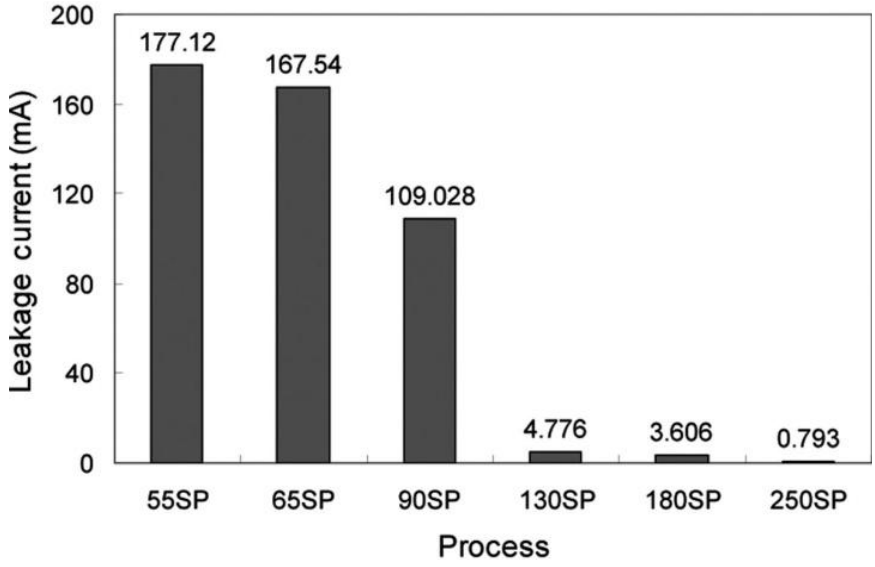


Figure 1. SRAM leakage current with technology scaling.

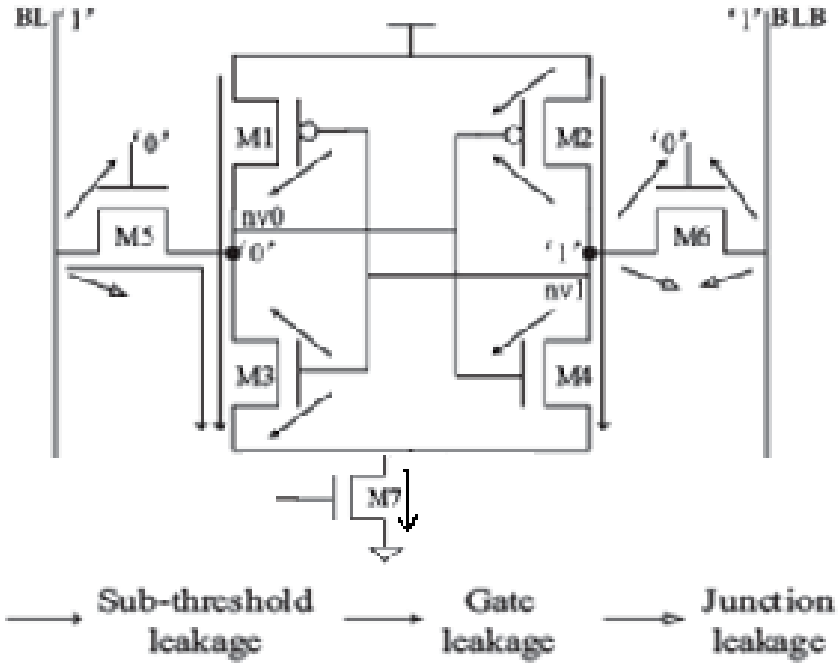


Figure 2. Leakage current in 7T SRAM cell.

doped halo doping profile (Razavipour et al., 2009), as shown in Figure 2.

Sub threshold leakage current

Sub threshold leakage current is the drain-source current of a transistor when the gate-source voltage is lower than the threshold voltage (Amelifard et al., 2008) and it is mainly composed of diffusion current. At present, the sub threshold leakage current still plays the main role in the three leakage mechanisms. There are two dominant sub threshold leakage paths in a 7T-SRAM cell as shown in Figure 2: (1) V_{DD} to the ground and (2) bit lines to the ground, through access transistors. When the node nv0 stores '0', there is significant sub threshold leakage

current through the off-transistors M1, M4, and access transistor M5, whereas, that of M6 is negligible, because its source-drain voltage difference is zero.

Gate leakage current

Reduction of gate oxide thickness results in an increase in the electric field across the oxide. Thus it leads to an exponential increase in tunneling probability of electrons through the gate oxide, and it means an exponential increase in the gate oxide tunneling current (Roy et al., 2003). As the gate leakage current of the positive-channel metal–oxide–semiconductor (PMOS) transistor is about one order of magnitude smaller than that of negative channel metal–oxide–semiconductor (NMOS), the gate leakage current mainly flows through the NMOS transistors M4, M5, and M6, and the mechanism is primarily edge direct-tunneling. Moreover, the gate leakage current of the on-transistor M3, that is primarily, direct tunneling, is the maximum.

Junction leakage current

The reversed biased Positive-channel, negative-channel (PN) junction leakage current has two main components: One corresponds to the minority carriers' diffusion near the edge of the depletion region, and the other is caused by an electron-hole pair generation in the depletion region of the reverse biased junction (Amelifar et al., 2008). It is an exponential function of doping concentration and reverse biasing voltage across the junction. Compared with other sources of leakage current, the junction current is quite small and mainly exists in access transistors M5 and M6, in a memory cell. Technology scaling, ultra-thin oxides and high doping concentrations have led to a rapid increase in gate leakage current and PN junction leakage current. The gate leakage current is even larger than the sub threshold leakage current from the 45 nm process downwards (Agarwal et al., 2006). Consequently, all the three leakage current components must be taken into account for standby leakage power reduction.

LEAKAGE POWER REDUCTION TECHNOLOGIES

There have been large varieties of techniques to deal with leakage power at different levels. In the device level, new material and process techniques have been introduced to control the channel length, oxide thickness, junction depth, and concentration distribution of transistors (Steegen et al., 2005; Koh et al., 2003; Zhao et al., 2004). An optimized Ni-Si process, a high angle, and low dose halo implants contribute to reduced junction leakage and gate-induced drain leakage (GIDL) current (Steegen et al., 2005). Novel transistor structures have been developed, for example, the Fin-Shaped Field Effect Transistor (FINFET), which has two or more gates to improve the gate control over the channel, leading to lower short channel effects and reduced sub threshold leakage current. Architectural level techniques such as multiple modes management have been presented, which put most unused memory sections into sleep or turn-off mode to achieve a large leakage current reduction (Kim et al., 2006; Flautner et al., 2002). Such a method is based on the fact that only a small fraction of SRAM works at a time. This article reviews some of the leakage power reduction techniques in circuit level for a 7T-SRAM cell (Verma, 2010; Chen et al., 2006; Heo et al., 2002). All of them are achieved by controlling different terminal voltages of the SRAM cell in standby mode. Figure 3 shows seven terminal voltages of a 7T-SRAM cell: V_{SL}, V_{DL}, V_{NWELL}, V_{PWELL}, V_{BL}, V_{BLB}, and V_{WL}. Between the impact of the techniques on the performance of the memory device such as static noise margin (SNM), and delay and area, the leakage current reduction must be traded off.

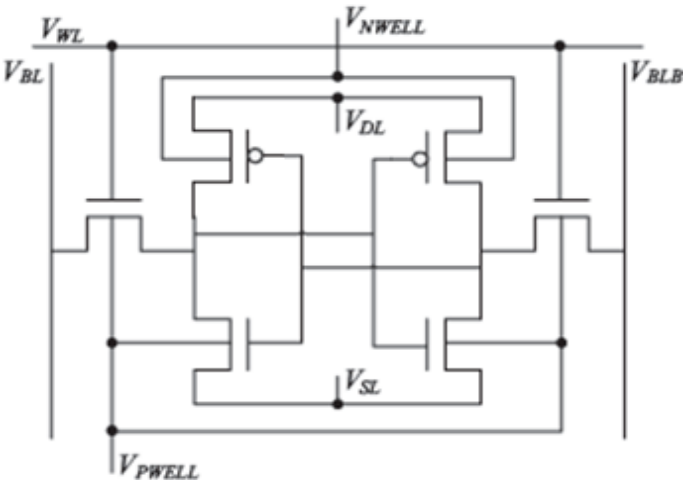


Figure 3. Seven terminal voltage of SRAM cell.

BODY-BIASING SCHEME

The body-biasing scheme is categorized as reverse body-biasing and forward body-biasing. They are adopted to reduce the leakage current on the basis that the sub threshold leakage current is exponentially dependent on the threshold voltage. As shown in Figure 4a, the reverse body-biasing scheme is applied by raising V_{NWELL} or lowering V_{PWELL} in the standby mode, to produce body effect and thus to increase the threshold voltage (Kim and Roy, 2002; Kawaguchi et al., 2001; Keshavarzi et al., 2001). Therefore, the sub threshold leakage current decreases with increasing V_{th}. In active mode, the body-biasing voltage is back to zero without affecting access time and data stability. However, extra

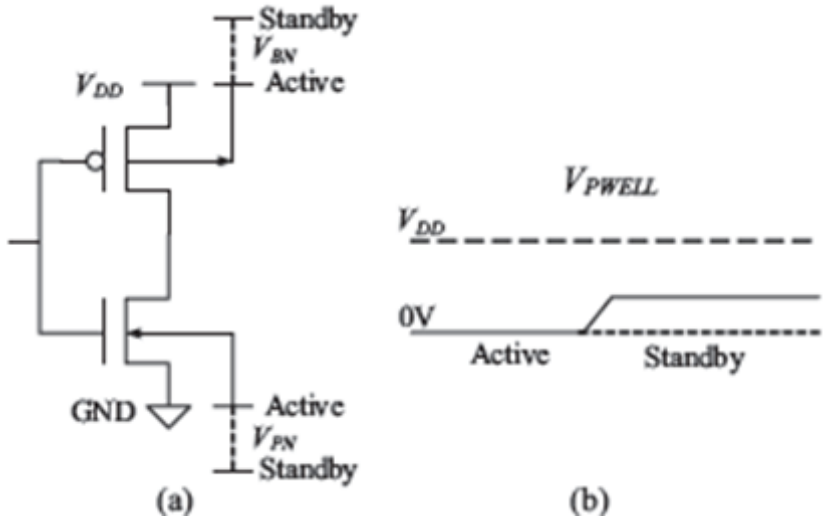


Figure 4. Body biasing scheme.

energy and time overhead must be taken into consideration owing to the body-biasing mode transition. The effectiveness of the reverse body-biasing scheme decreases with technology scaling, due to worsening of the body effect caused by the shorter channel length. In addition, source-substrate, drain-substrate leakage current, and band-to-band tunneling current exponentially increase at the source-substrate and drain-substrate PN junctions (because of halo doping in scaled devices) (Agarwal et al., 2006). The simulation results have also proved it. In Kim and Roy (2002), the author proposed a dynamic V_{th} SRAM in which the body-biasing voltage of NMOS transistors was raised to V_{th} for the cells not likely to be accessed anymore. The simulation results demonstrated that a leakage current of 64 KB L_1 instruction cache can be saved by 72% at 0.18 µm technology. In contrast to the reverse body-biasing scheme, the forward body-biasing scheme raises V_{PWELL} for selected SRAM cells, to increase the threshold voltage in the active mode so as to achieve fast operation (Razavipour et al., 2009; Kim et al., 2005, Hamzaoglu et al., 2009). High V_{th} devices built by high channel doping have been used to reduce the leakage current in the standby mode. Process complexity increases for high channel doping, where leakage mechanisms in the nanometer regime are considered. Both forward body biasing and high channel doping can improve device performance, suppressing the short channel effect and V_{th} roll-off. Therefore, the forward body-biasing scheme is more applicable as a technology scale. However, they have larger junction capacitance and body effect, which reduces the delay improvement, especially in stacked circuits (Agarwal et al., 2006).

The forward body-biasing scheme (raising V_{PWELL} to 0.5 V) and super high V_{th} (350 mV) devices, to reduce cache leakage power, have been used in the study of Kim et al. (2005). In the case of 1.0 V supply voltage and 270 mV normal device threshold voltages, 64% leakage power reduction can be achieved for a 32 KB L_1 cache. A design can use the reverse body-biasing scheme in standby mode to reduce leakage current together with the forward body-biasing scheme in active mode for high performance, which is more effective than if only one of them is used in the design. Researchers have found that forward body-biasing and high V_{th} devices along with the reverse body-biasing scheme provide 20 times the leakage reduction, as opposed to three times the leakage reduction for the reverse body-biasing and low V_{th} devices (Agarwal et al., 2006).

SOURCE BIASING SCHEME

The source biasing scheme raises the ground voltage V_{SL} in the standby mode (Razavipour et al., 2009; Agarwal and Roy, 2003; Elakkumanan et al., 2003), which produces a similar effect as the stacking effect, to achieve a large reduction in the leakage current.

Generally, a pull-down NMOS transistor M7is inserted between the ground (GND) and source lines of the SRAM cell (Agarwal et al., 2003; Hua et al., 2005; Lee et al., 2007). As shown in Figure 5, its gate terminal is connected to the word line (WL). In active mode, the WL goes high and then M7 is turned on. As its resistance is very small, the virtual ground voltage V_{SL} almost functions as the real ground line and the SRAM cell works conventionally. In standby mode, WL is set low and M7 is turned off, thus raising the source voltage and reducing both the sub threshold and gate leakage current. The raised source voltage V_{SL} produces body effect, as the substrate voltage remains a constant. Hence, the threshold voltage increases, associated with the reduced

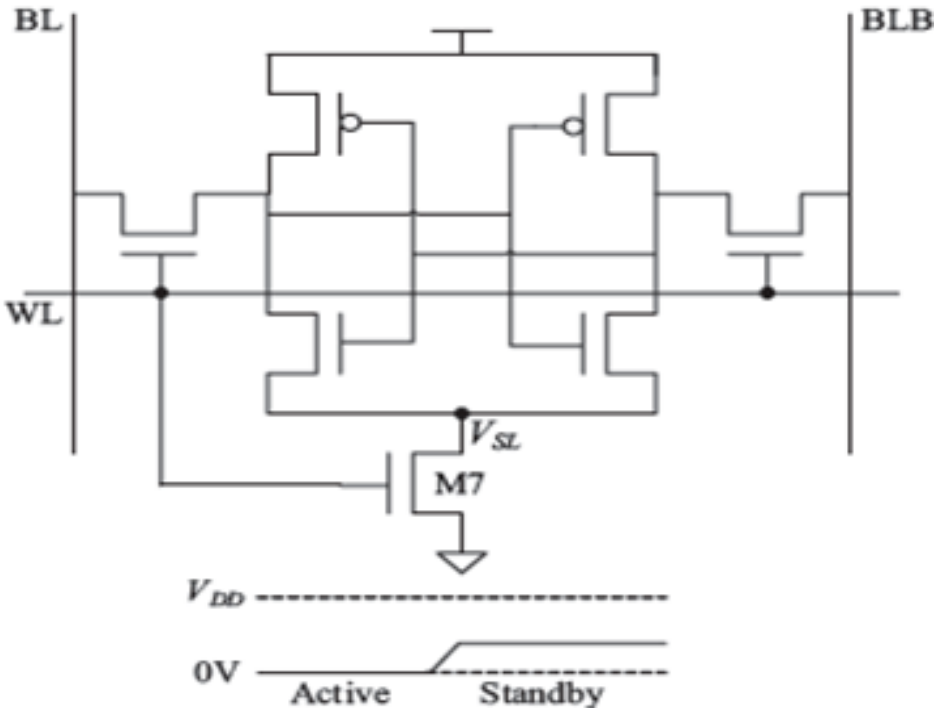


Figure 5. Source biasing scheme.

signal rail ($V_{DD} – V_{SL}$), and then the sub threshold leakage current is lowered. The reduced voltage difference between the drain and source terminals results in a lower drain-induced barrier lowering (DIBL) effect and also reduces sub threshold leakage current. At the same time, the gate leakage current also decreases due to the reduced potential of gate-source, gate-drain, and gate-substrate of most transistors in the SRAM cell. One drawback of this scheme is that the extra transistor M7 in the pull-down path will get a delay penalty, increasing both area and dynamic energy consumption. To minimize the area overhead, the pull-down transistor is often shared by a bank of SRAM cells. Moreover, the reduced rail-to-rail voltage results in an increased soft error rate (SER), which requires additional error correction coding circuits (Kim et al., 2005). Considering the data retention capability in the standby mode, the sizing and threshold voltage must be carefully controlled and between them the leakage current saving should be traded off. An IWL-VC SRAM has been proposed in the study of Razavipour et al. (2009), which reduces the sub threshold leakage current by increasing the ground level during idle time with two NMOS transistors. Gate leakage current of access transistors is also lowered by the increasing word line voltage from V_{SS} to V_{th} of the PMOS-controlled transistor. Simulation results for a 45 nm technology, with an oxide thickness of 1.4 nm shows that the total gate leakage current and standby power are decreased by 66 and 58%, respectively, with approximately 2% access time penalty.

DYNAMIC V_{DD} SCHEME

The dynamic V_{DD} scheme presented in the study of Fukano et al. (2008) and Martin et al. (2002) is available in the state-of-the-art SRAM design. In active mode, normal supply voltage is applied to a conventional read / writes operation, without delay penalty. Reducing supply voltage in the standby mode effectively decreases the sub threshold, gate, and junction leakage current. However, the reduced supply voltage results in a lower static noise margin and possible data flipping failures. On the other hand, extra peripheral circuitry such as a high efficiency voltage converter is required and a significant wake-up access time and dynamic power latency are introduced, with respect to the conventional SRAM cell, when switching between different modes. Besides, the greatest drawback is the substantial increase in the SER, with voltage scaling (Kim et al., 2005).

Cell stability is becoming a great challenge with the scaling of technology. We must guarantee data retention capability, while leakage power reduction is obtained. Data retention voltage (DRV) defines the minimum standby voltage as that under which the SNM of a memory cell equals to zero and the data is still preserved (Qin et al., 2004). It is a strong function of process variations, transistor size, temperature, and so on. The DRV of a full SRAM array produces a set of normally distributed random values caused by variations in the process and global environment. Thus the worst-case tail of DRV distribution determines the chip yield (Wang et al.

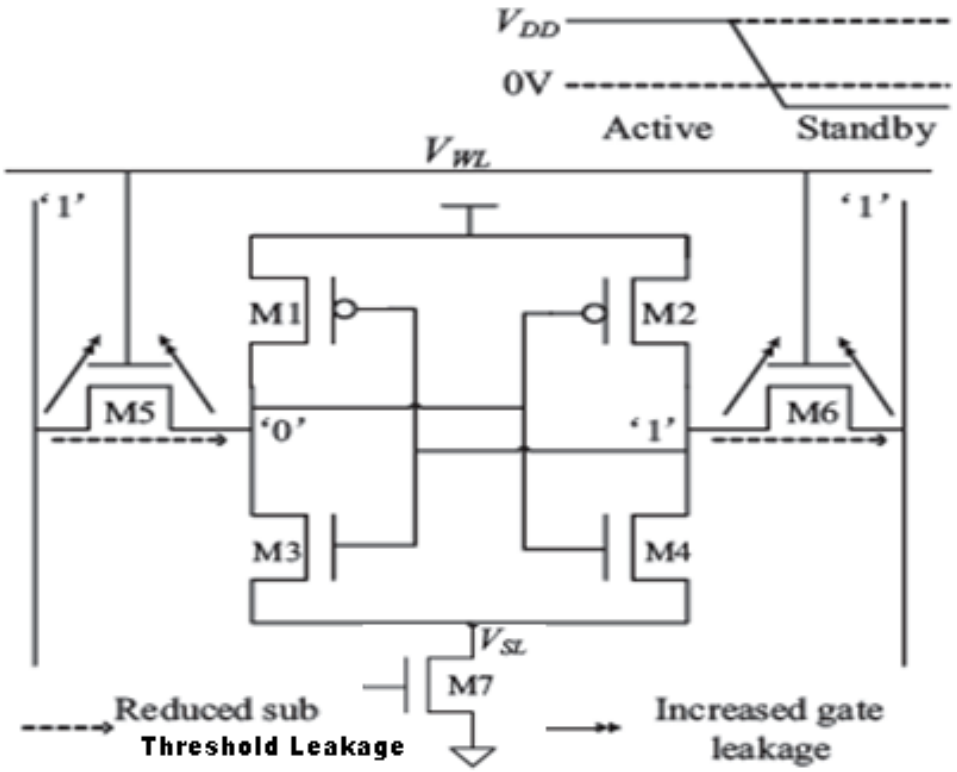


Figure 6. Negative word line scheme.

., 2007). An optimal standby V_{DD} not only preserves cell data, but also greatly reduces the leakage current. Test results presented in the study of Qin et al. (2004) from a 90 nm SRAM test chip, with a 400 mV reverse body-biasing voltage and 50% device channel length increase, indicating that a 270 mV standby V_{DD} is demonstrated, leading to a 97% leakage power reduction. However, it adds a guard-band voltage to the worst-case standby V_{DD} for sufficient static noise margin, which may waste large leakage power saving for non-worst-case conditions. A canary-based feedback loop to sense the proximity of the currently applied V_{DD} to the DRV of the overall SRAM cells by tracking PVT variations through canary cell failures has been proposed in the study of Wang and Calhoun (2008). Power saving of a 90 nm 128 KB SRAM test chip improves up to 30 times compared with the guard-banding approach.

NEGATIVE WORD LINE

The negative word line scheme is utilized to generate a negative voltage supplied to the word line during idle time (Kanda et al., 2002, Itoh et al., 1996) without affecting the device performance or SER. The sub threshold leakage current of access transistors is reduced, as they are strongly turned off. At the same time, the gate leakage current of access transistors increases as a result of enlarged gate-source and gate drain voltage differences as shown in Figure 6. Just like the dynamic V_{DD} scheme, there is dynamic power overhead and an extra voltage generator needed for providing the negative voltage.

A novel SRAM in which word line voltage is supplied with -0.2 V in standby mode, combined with a dynamic V_{DD} scheme (0.2 V standby supply voltage) has been proposed in the study of Kanda et al. (2002).

BITLINE FLOATING

As shown in Figure 2, the leakage current from bit lines to access transistors depends on the storing data of the corresponding node. When the voltage of bit line (BLB) equals to the storing value (nv1), the source-drain voltage difference of the access transistor (M6) is zero, and thus its sub threshold leakage current is negligible. Consequently, BL is set at zero and BLB is kept high if the node nv0 of all memory cells store '0,' to reduce bit line leakage current. On the contrary, if the node nv0 of all memory cells store '1', we force BLB to a zero value, while keeping BL pre-charged. Generally, '0' and '1' always coexist at the same time in the chip. A technique that turns off pre-charge transistors and allows the bit lines to float in a standby mode is proposed, to reduce the leakage current of access transistors via the DIBL effect. Although the bit lines are left floating, they are

disconnected from the sense-amplifier by the column-mux and there is no new leakage path introduced. As bit lines must be pre-charged to V_{DD} for the read / write operation, an extra pre-charge cycle is required, while switching back to active mode, which leads to a speed latency. The bit line floating scheme is applied in the study of Heo et al. (2002) to reduce the leakage current. It saves over 24% leakage power of I-cache memories and nearly 50% of the register file when using a 70-nm process.

SIMULATION RESULTS

In this section, we present simulation results on the leakage energy savings, static noise margin, and read-current of the above leakage power reduction techniques, based on the UMC 45 nm CMOS process. They are analyzed for the different control terminal voltages of each technique. Figures 7 to 12 show detailed results for different process corners and temperatures, where the leakage saving ratio is the rate of original leakage current to reduced leakage current. The lower the read-current, the larger the delay. T, F, and S in the figures are short for typical, fast, and slow MOS transistors, respectively. For example, PFNF - 40 means the simulation condition of fast PMOS and fast NMOS at a temperature of - 40°C. We have not simulated the forward body-biasing scheme on account of limited conditions. Figures 7 and 8 present two ways of reverse body-biasing: Raising V_{NWELL} and lowering V_{PWELL}. As shown in Figures 7a and 8a, a higher reverse body-biasing voltage leads to a larger reduction in leakage current and it is obvious that the effectiveness of the leakage suppressing capability is better at the PFNF process corner. Raising V_{NWELL} to 1.4 V provides the maximum leakage saving (1.18 times) at the condition of PFNF 25°C, while 1.46 times leakage power reduction is achieved for -0.4 V NMOS body-biasing voltage at PTNT 125°C. However, the leakage current even increases in some cases such as PTNT-40, PSNS -40, and PSNS 25. Referring to the memory performance, static noise margin and read-cur-rent almost keep the same, with raised V_{NWELL}, whereas, reducing V_{PWELL} increases hold-SNM and decreases read-current slightly, thus, access time increases a bit. Generally speaking, the reverse body-biasing scheme has little effect on SRAM cell stability and delay time. Figures 9 and 10 show the impact of dynamic V_{DD} and the source biasing schemes on the leakage saving and read-current. They have a similar effect owing to the equivalent reduced signal rail. Compared with the results in the reverse body-biasing scheme, a dramatic reduction in the leakage current is attained due to the reduction all of three leakage components, at the cost of decreased SNM, and increased delay. When the source voltage is raised to 0.4 V, the leakage current is reduced by a factor of 8.16 at the condition of PTNT -40°C, similar to the effect of reducing

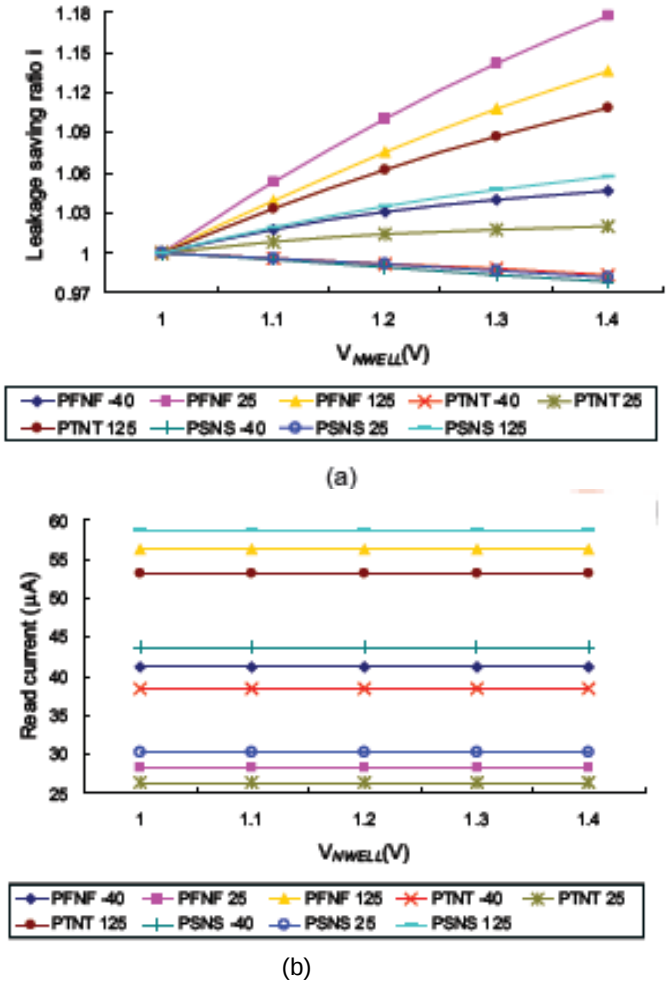
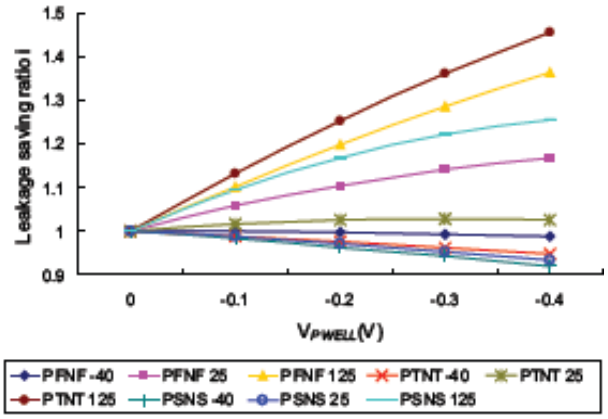


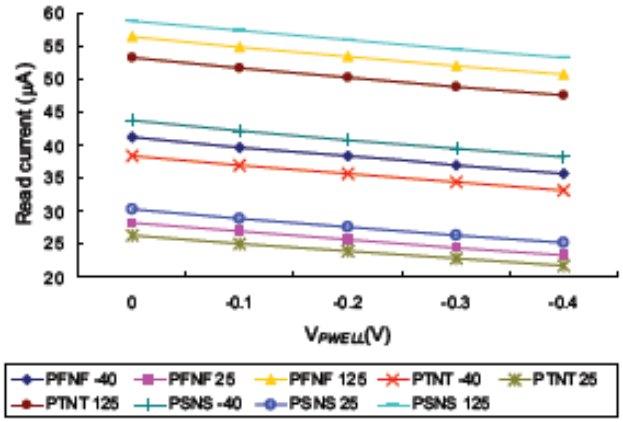
Figure 7. (a) Raising v_{NWELL} effects on SRAM cell standby leakage current; (b) Raising v_{NWELL} effects on read current of SRAM cell.

standby V_{DD} to 0.6 V. Figure 9 indicates that 0.5 V standby V_{DD} obtains maximum (15.8 times) leakage energy saving, but reduces hold-SNM to only 169.2 mV, which may cause retention data flipping failures. SRAM cell delay is now almost ten times its original value. To reduce standby voltage further, without cell failures, enlarging transistor channel length is a feasible way to decrease DRV at the price of area overhead (Qin et al., 2004). The effects of negative word line and bit line floating schemes on reduction in the leakage current are presented in Figures 11a and 12a.

As only the access transistors benefit from the techniques, the overall leakage savings are marginal. When a negative voltage of -1.2 V is applied to the word line in standby mode, maximum leakage current reduction (1.22 times) is obtained at the condition of PTNT 125°C. However, the phenomenon of leakage current increase is observed at PTNT-40, PSNS-40, and PSNS-25, because the increased gate leakage current of access transistors

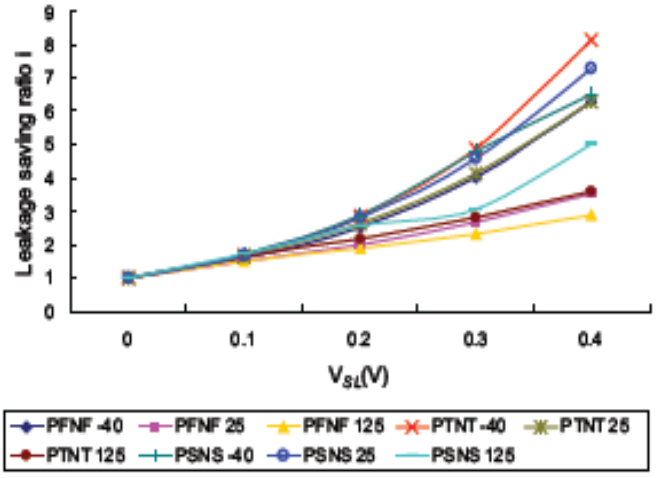


(a)

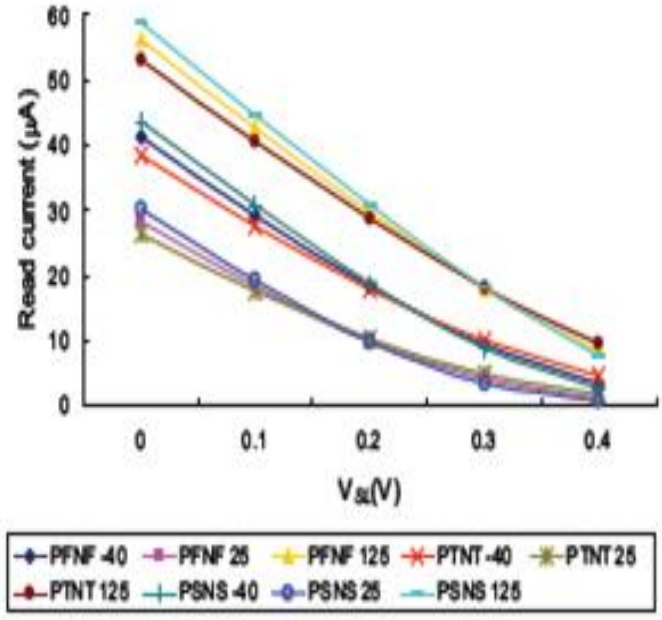


(b)

Figure 8. (a) Reducing V_{PWELL} effects on SRAM cell standby leakage current; (b) Reducing V_{PWELL} effects on read current of SRAM cell.



(a)



(b)

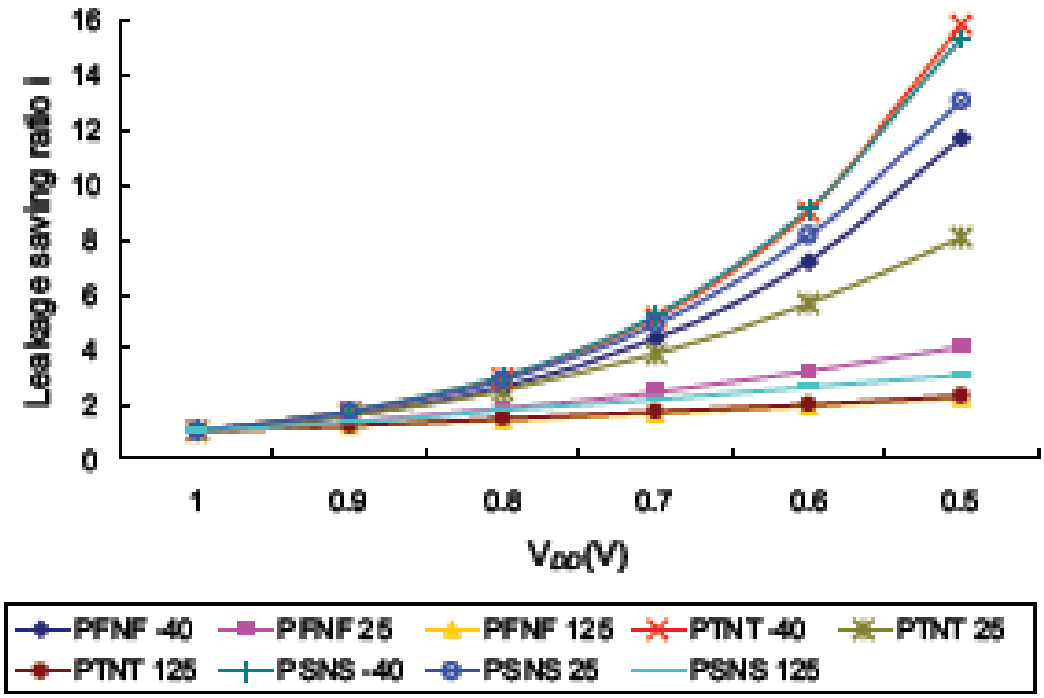
Figure 9. (a) Source biasing scheme effects on SRAM cell standby leakage current; (b) Source biasing scheme effects on read current of SRAM cell.

here is larger than the decreased sub threshold leakage current. As shown in Figure 12a, the leakage suppressing capability of the bit line floating scheme improves with increased temperature and also gets the maximum (1.25 times) at the condition of PTNT at 125°C. In addition, the memory performance has not been greatly affected by negative word line and bit line floating schemes.

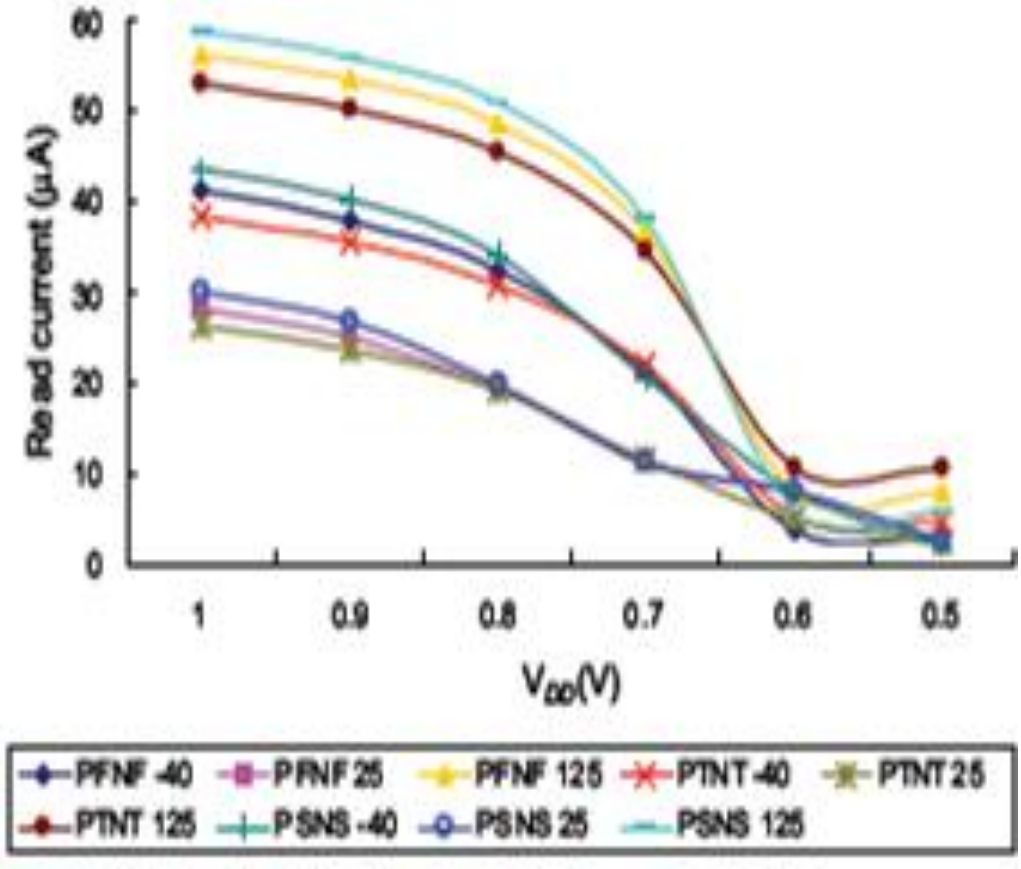
On the basis of the simulation results, the effects of body biasing, source biasing, dynamic V_{DD}, negative word line, and bit line floating schemes on the leakage current reduction, data stability, and cell delay have been given in Table 1. From the viewpoint of leakage current reduction, data stability, and cell delay, different techniques have different advantages and disadvantages.

Conclusion

Static random access memory standby leakage power has become a major issue in modern low power SOC devices with technology scaling. This article summarizes the existing leakage reduction techniques, including body biasing, source biasing, dynamic V_{DD}, negative word line, and bit line floating schemes. We have also compared them based on simulation results and they have demonstrated that different techniques have different advantages and disadvantages. In a word, dynamic V_{DD} and source biasing schemes show greater leakage suppressing capability, whereas, the static noise margin of the other techniques almost keeps the same. As a result, SRAM cell optimization must be seeking a tradeoff between power consumption and device performance.

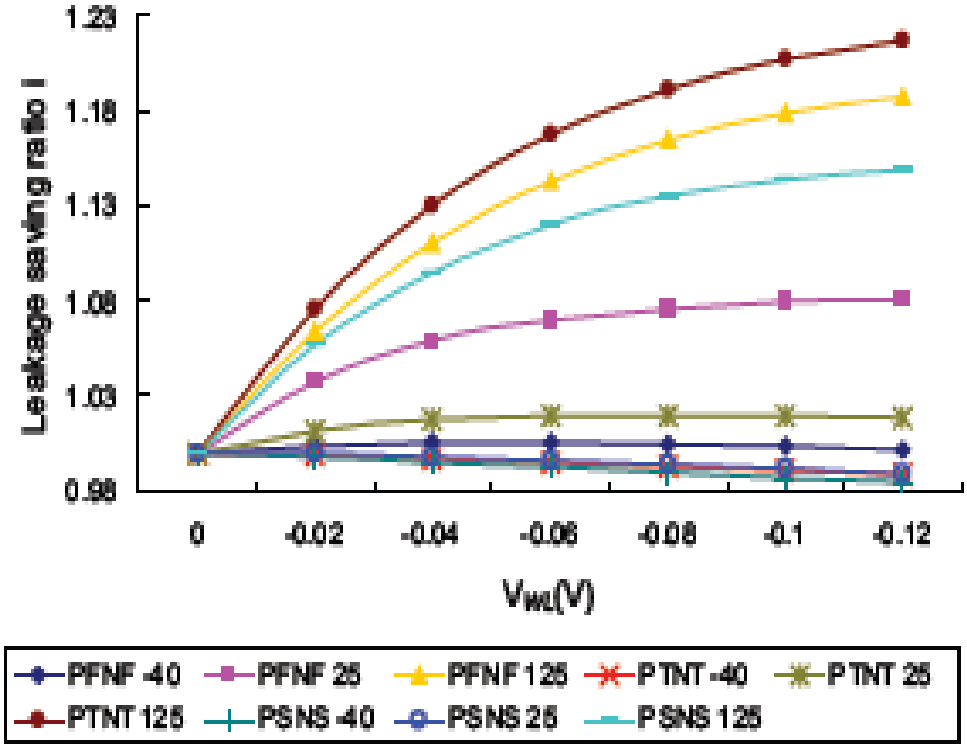


(a)

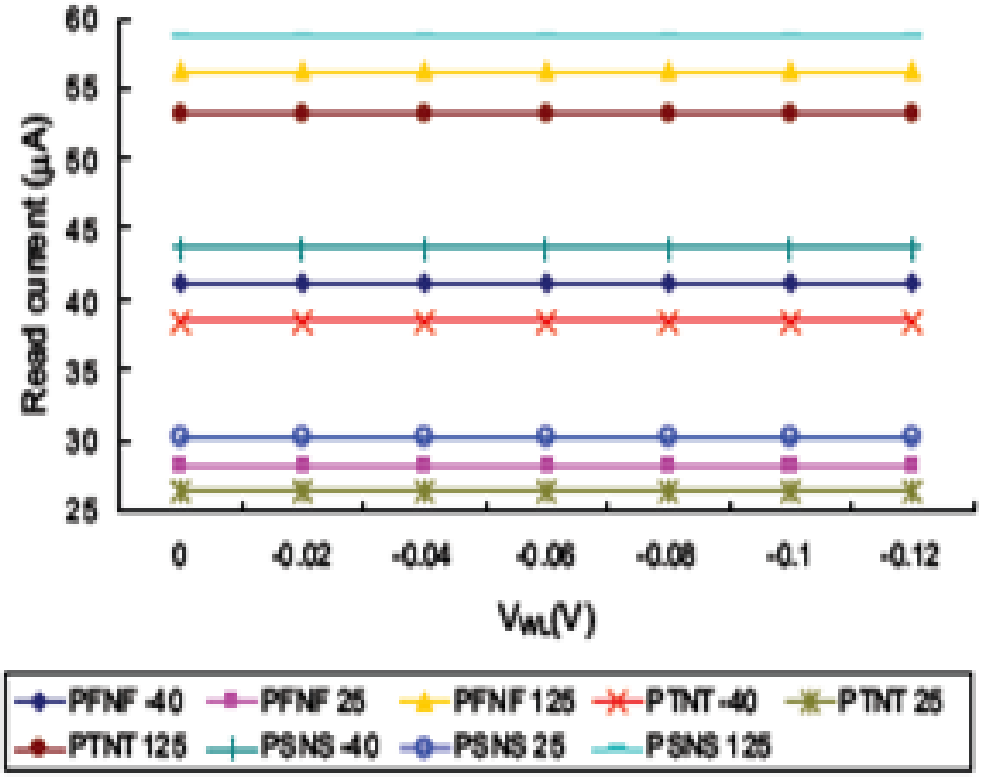


(b)

Figure 10. (a) Dynamic V_{DD} scheme effects on SRAM cell standby leakage current (b) Dynamic V_{DD} scheme effects on read current of SRAM cell.



(a)



(b)

Figure 11. (a) Negative word line scheme effects on SRAM cell standby leakage current; (b) negative word line scheme effects on read current of SRAM cell.

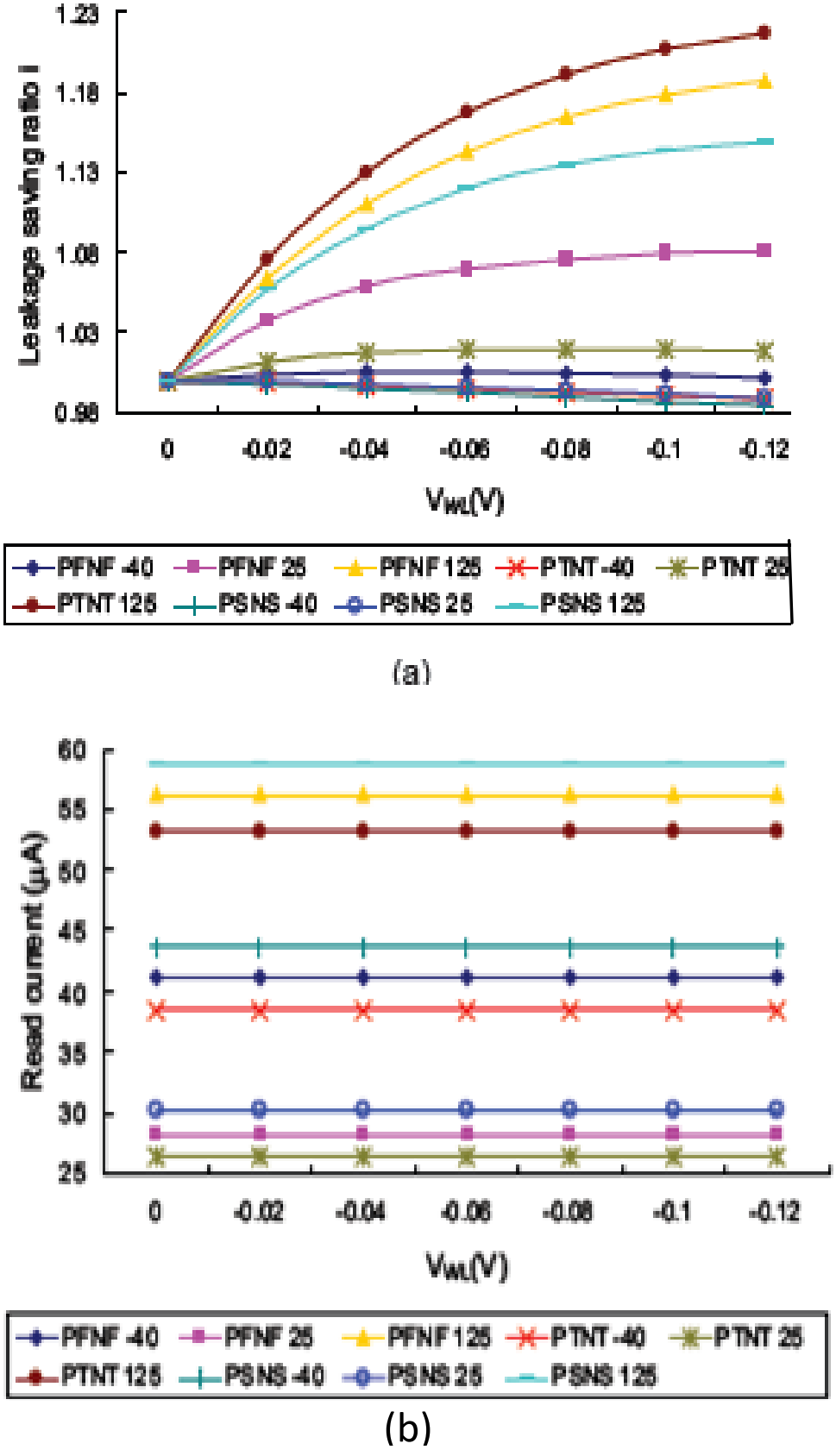


Figure 12. (a) Bit line floating scheme effects on SRAM cell standby leakage current; (b) bit line floating scheme effects on read current of SRAM cell.

Table 1. Comparison of different SRAM leakage power reduction techniques.

Low power techniques	Leakage	Delay	Drawback
Reverse body bias	Sub threshold leakage decreases while junction leakage increases	Almost keeps the same	The effectiveness reduces with technology scaling
Forward body biasing combined with high- V_{th} devices	Sub threshold leakage decreases	Increases a little	More complex process
Source biasing scheme	Sub threshold, gate, and junction leakage all decrease	Increase	Dynamic power and SER increases
Dynamic V_{DD}	Sub threshold, gate and junction leakage all decrease	Increase	Extra voltage converter
Negative word line	Sub threshold leakage decreases while gate leakage increases	Almost keeps the same	Dynamic power increases
Bit line floating	Sub threshold and gate leakage of access transistors decrease	Decreases a little	An extra pre-charge cycle is required.

REFERENCES

Agarwal A, Roy K (2003). A noise tolerant cache design to reduce gate and sub-threshold leakage in the nanometer regime. Proceedings of the 2003 International Symposium on Low Power Electronics and Design, pp.18-21.

Agarwal A, Li H, Roy K (2003). A single-V_t low-leakage gated-ground cache for deep submicron", IEEE J., 38: 319-328.

Agarwal A, Mukhopadhyay S, Raychowdhury A, Roy K, Kim CH (2006). Leakage power analysis and reduction for nanoscale circuit. Micro IEEE, 26: 68-80.

Amelifard B, Fallah F, Pedram M (2008). Leakage minimization of SRAM cells in a dual-V and dual-T technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 16: 851-859.

Chen Q, Mukhopadhyay S, Bansal A, Roy K (2006). Circuit- aware device design methodology for nanometer technologies: A case study for low power SRAM design. Proceedings Design, Automation and Test Munich, pp. 1-6.

Elakkumanan P, Narasimhan A, Sridhar R (2003). NC-SRAM – a low-leakage memory circuit for ultra deep submicron designs. Proceedings International SOC Conference, pp. 3-6.

Flautner K, Kim NS, Martin S, Blaauw D, Mudge T (2002). Drowsy caches: Simple techniques for reducing leakage power. Proceedings 29th Annual International Symposium on Computer Architecture, Anchorage, AK, pp. 148-157.

Fukano G, Kushida K, Tohata A, Takeyama Y, Imai K, Suzuki A (2008). A 65nm 1Mb SRAM macro with dynamic voltage scaling in dual power supply scheme for low power SoCs. International Conference on Memory Technology and Design, Opio, pp. 18-22.

Hamzaoglu F, Zhang K, Wang Y, Ahn HJ, Bhattacharya U, Chen Z (2009). A 3.8GHz 153Mb SRAM Design with Dynamic Stability Enhancement and Leakage Reduction in 45 nm High-k Metal Gate CMOS Technolog. IEEE J. Solid-State Circuits, 44: 148-154.

Heo S, Barr K, Hampton M, Asanoví´c K (2002). Dynamic fine-grain leakage reduction using leakage-biased bitlines. Proceedings of the 29th Annual International Symposium on Computer Architecture, Anchorage, AK, USA, pp. 137-147.

Hua C, Cheng T, Hwang W (2005). Distributed data-retention power gating techniques for column and row co-controlled embedded SRAM. IEEE International Workshop on Memory Technology, Design, and Testing, Taipei, pp. 129-134.

Itoh K, Fridi AR, Bellaouar A, Elmasry MI (1996). A deep sub-V, single power-supply SRAM cell with multi-Vt, boosted storage node and dynamic load. Proceedings Symposium on VLSI Circuits, Honolulu, HI, pp. 132-133.

Kanda K, Miyazaki T, Sik MK, Kawaguchi H, Sakurai T (2002). Two orders of magnitude reduction of low voltage SRAM's by row- by-row dynamic V control (RDDV) scheme. Proceedings of IEEE International ASIC/SOC Conference, NY, USA, pp. 381-385.

Kawaguchi H, Itaka Y, Sakurai T (2001). Dynamic leakage cut- off scheme for low-voltage SRAM. Symposium on VLSI Technology Digest of Technical Papers, Honolulu, HI, pp. 140-141.

Keshavarzi A, Ma S, Narendra S, Bloechel B, Mistry K, Ghani T (2001). Effectiveness of reverse body bias for leakage control in scaled dual Vt CMOS ICs. International Symposium on Low Power Electronics and Design, Huntington Beach, CA, pp. 207-212.

Kim CH, Kim JJ, Chang IJ, Roy K (2006). PVT-aware leakage reduction for on-die aches with improved read stability. IEEE J. Solid-State Circuits, 41: 170-178.

Kim CH, Kim JJ, Mukhopadhyay S, Roy K (2005). A forward body-biased low-leakage SRAM cache: device circuit and architecture considerations. IEEE Trans. VLSI Syst., 13: 349-357.

Kim CH, Roy K (2002). A leakage tolerant cache memory for low voltage microprocessors. Low Power Elect. Design, pp. 251-254.

Koh K, Hwang BJ, Kwak KH, Son YS, Lee JY, Jang JH (2003). Highly manufacturable 100nm 6T low power SRAM with single poly-Si gate technology. International Symposium on VLSI Technology, Systems, and Applications, pp. 64-67.

Lee DH, Kwak DK, Min KS (2007). Comparative study on SRAMs for suppressing both oxide-tunneling leakage and subthreshold leakage in sub-70-nm leakage dominant VLSI. 20th International Conference on VLSI Design, Bangalore, pp. 632-637.

Martin SM, Flautner K, Mudge T, Blaauw D (2002). Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads. IEEE/ACM Int. Conf. Comput. Aided Design, pp. 721-725.

Qin H, Cao Y, Markovic D, Vladimirescu A, Rabaey J (2004). SRAM leakage suppression by minimizing standby supply voltage. Proceedings 5th International Symposium on Quality Electronic Design, San Jose, CA, USA, pp. 55-60.

Razavipour G, AfzaliKusha V, Pedram M (2009). Design and analysis of two low power SRAM cell structure. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17: 1551-1555.

Roy K, Mukhopadhyay S, Mahmoodi H (2003). Leakage current

mechanisms and leakage reduction techniques in deep sub-micrometer CMOS circuits. Proceedings of the IEEE, 91: 305-327.
Steegen A, Mo R, Mann R, Sun MC, Eller M, Leake G, Vietzke D (2005). 65nm CMOS technology for low power applications. IEEE International Electron Devices Meeting, Washington, DC. pp. 64-67.
Verma N (2010). Analysis towards minimization of total SRAM energy over active and idle operating modes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 99: 1-9.
Wang J, Calhoun B (2008). Techniques to extend canary-based standby V scaling for SRAMs to 45 nm and beyond. IEEE J. Solid-State Circuits, 43:2514-2523.
Wang J, Singhee A, Rutenbar RA, Calhoun BH (2007). Statistical modeling for the minimum standby supply voltage of a full SRAM array. 33rd European Solid State Circuits Conference, Munich, pp. 400-403.
Zhao S, Chatterjee A, Tang S, Yoon J, Crauk S, Bu H (2004). Transistor optimization for leakage power management in a 65nm CMOS technology for wireless and mobile applications. Symposium on VLSI Technology Digest of Technical Papers. pp. 14-15.