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Full Length Research Paper

Adjustable filtering structure design dedicated to a programmable hearing aid apparatus

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This research concerns the conception and the development of one specific circuit for a programmable hearing aid. In fact, actual hearing aid prosthesis should be flexible and programmable apparatus to the pathological case. First of all, it must be adjusted according to the pain threshold conserving all dynamics sound. Second, it must be adapted to different patient audiogram levels. In this article, we present the design of our conception using an adjustable amplifying chain formed by five analogue filters. In particular, such filters could be adjusted according to patient audiogram in order to compensate the considered hearing loss. Amplifier structure in this filters' chain were independently controlled using current sources conceived by MOS transistors. At each amplifying structure, one could distinguish two stages referred as A_{mg} and A_{mf} : A_{mg} was conceived to control the filter's gain where A_{mf} was conceived to control frequency band width. On the other hand, one MOS transistor current source was commanded by a Digital to Analogue Converter assuring then the possibility of programmability. The overall circuit was conceived using MOS technology in order to satisfy the low power incessant need for such biomedical applications.

Key words: Programmable hearing aid, Filter, Amplifier, Digital to Analogue Converter.

INTRODUCTION

Research in deafness rehabilitation field became one real necessity in our common life (Karen, 2000; Sterkers et al., 1982). Indeed, this handicap is a real and serious problem causing social disintegration of a wide percent of the active society. Hearing aid apparatus were intended for persons suffering from mild to deep deafness where simple medical treatments were ineffective. Some apparatus are former as ones used in conventional hearing aids which bring a simple amplification of sounds. But a simple amplification of sounds became really insufficient regarding patient needs. That's why one must give flexible solution for achieving a convenient level of adaptability (Serdijn et al., 1995).

Our biomedical research group was very interested in the conception and in the development of a specific circ uit for one programmable hearing aid apparatus. Actual hearing aid prosthesis should be flexible and programmable apparatus in order to be adaptable to the pathological case (Nunley, 1983). First of all, it must be adjusted according to the pain threshold conserving all dynamics sound. Second, it must be adapted to different patient audiogram levels. For our design, the adjustment involves digital information transfer from PC to the apparatus' memory (EPROM).

In this conception, we used a convivial structure based on an adjustable amplifying chain formed by five analogue filters. In particular, such filters could be adjusted according to patient audiogram in order to compensate the considered hearing loss.

The amplifying structure of these filters was essentially based on independently controlled current sources conceived by MOS transistors. At each amplifying stage, we proposed two independent stages (A_{mg} and A_{mf}) for controlling either the gain as well as the frequency band width. The overall circuit was conceived using MOS technology in order to satisfy the low power incessant need for such biomedical applications (Serdijn et al., 1995).

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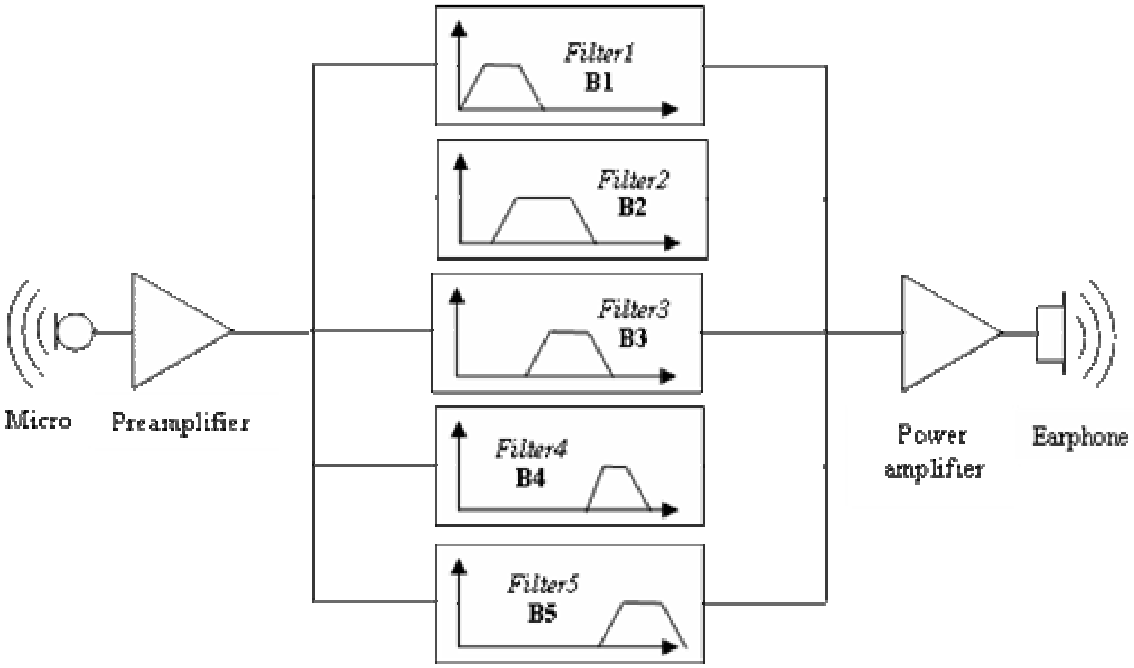

Figure 1. Hearing prosthesis programmable filtering structure.

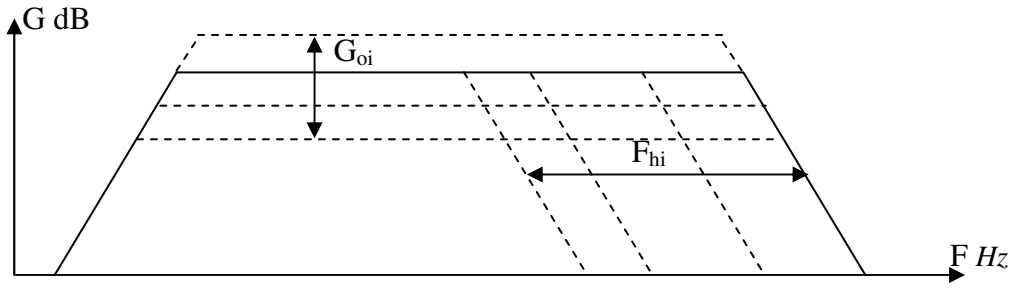

Figure 2. Programmable analogue filter: Adjustment of G_{oi} and F_{hi}.

The paper was structured as follows: we propose first of all the programmable hearing aids' structure to be conceived. We explain the amplification structure relatively to one filtering stage, which includes two independent amplification modules referred to as A_{mg} and A_{mf}. Then, we present the digital to analogue converter (DAC), and finally the complete filtering structure of our proposed hearing aid circuit.

Programmable hearing aids' structure

As mentioned above, general signal processing structure of one programmable hearing aid prosthesis consists essentially of an amplification structure composed of two control modules A_{mg} and A_{mf}. The mere objective is to adapt such programmable device to the already experimented audiogram (Chaoui et al., 2002). This signal is amplified then directed towards an ear-phone placed in the ear. The structure of the programmable hearing aid, proposed for the design, is represented by Figure 1.

The principle of this hearing prosthesis consists in dividing the audible frequency domain clinically considered from 50Hz to 8000Hz into five arbitrary bands as illustrated in Figure 1 (Ghariani et al., 2001). At each active band pass filter with a fixed low cut-off frequency F_{bi}, the gain G_{oi} and the high cut-off frequency F_{hi} would be adjustable in order to provide the desired program-mability (Figure 2). Finally, we will have five identical electronic stages placed in parallel receiving the preamplified

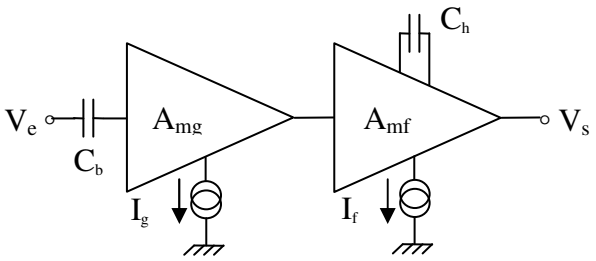

Figure 3. Amplification structure.

microphone signal and delivering the programmable filtering to the ear phone. In fact, the output filtered signals will issued from each programmable filter would be mixed thanks to an appropriate mixing amplifier.

Amplification structure: One filtering stage

Each amplifying structure provided for one filtering stage must be able to control independently the gain G_{oi} by a current source structure (by means of I_g), and the high cut-off frequency F_{hi} by another current source (by means of I_f). A capacity C_b fixes the low cut-off frequency F_{bi}. Moreover, one capacity C_h is added to fix the first value F_{ho} of each stage as shown in Figure 3.

We will be interested in the study and the design of these A_{mg} and A_{mf} amplificatory cells. These two stages where totally commanded by MOS current sources.

A_{mg} Amplification module characteristic

A_{mg} amplification module is based on one differential amplifier structure produced by two identical transistors M_1 and M_2 (Figure 4). The two transistors' group (M_3, M_5, M_7) and (M_2, M_4, M_6) constitute respectively the active load of M_1 and M_2 transistors permitting to fix the stage gain $A = -g_m R$, where R is the equivalent resis-tance of each group of transistors.

For these transistors, regarding low V_{DS} values which corresponds to the unsaturated area (ohmic area) relative to ($|V_{DS}| \leq |V_{GS}| - |V_T|$), the device would be equivalent to one resistance where its value depends on V_{GS} voltage. For small signals, the channel resistance r_{ds}, given by the following equation (1) (Allen et al., 2002), would be considered as an active charge of the considered amplifier and couldn't depend on polarization current I_g.

$$r_{ds} = \frac{L}{K'W(V_{sg} - V_T - V_{ds})} \quad (1)$$

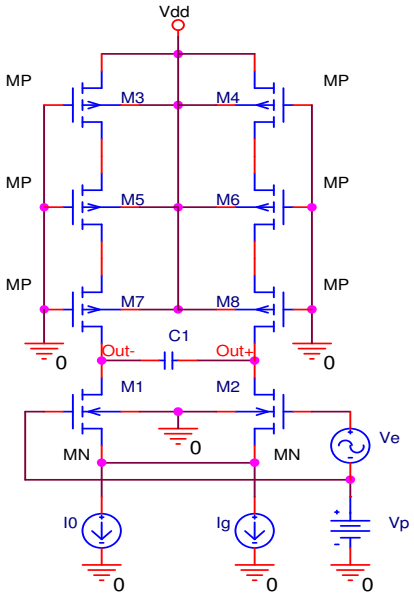

Figure 4: A_{mg} Amplification module: MOS active charge.

Where L is the channel length, W is the channel width, V_T is the threshold voltage and K' is the transconduc-tance parameter.

In order to operate in the linear zone of the transfer characteristic of this differential amplifier, an appropriate active charge r_{ds}=30KΩ could be considered for M_1 as well as for M_2. (Yaïch, 2004). This was one reason to place three identical transistors in series, considering an equivalent resistance of 10KΩ for each transistor.

The A_{mg} command current I_g would be scaled from 0 to 64µA at ΔI=2µA step thanks to an appropriate technique (Ghariani, 2006). The current source I_0 would be added in order to generate a pre-polarisation current of 2µA.

The gains' ratio corresponding to the control current (I_g) could be expressed by (Gray, 1982):

$$\frac{A_{\max}}{A_0} = \frac{g_m R}{g_{m0} R} = \frac{\sqrt{\beta(I_{g\max} + I_0)}}{\sqrt{\beta I_0}} = 5.6 \quad (2)$$

This corresponds to a dynamics of 15dB.

Where A_0 and A_{0max} are the gains obtained relatively to the minimum current I_0 and to the maximum current I_{gmax} (I_{gmax}=64µA, I_0=2µA).

g_m and g_{m0} are the channel conductances, and

$$\beta = K' \frac{W}{L}.$$

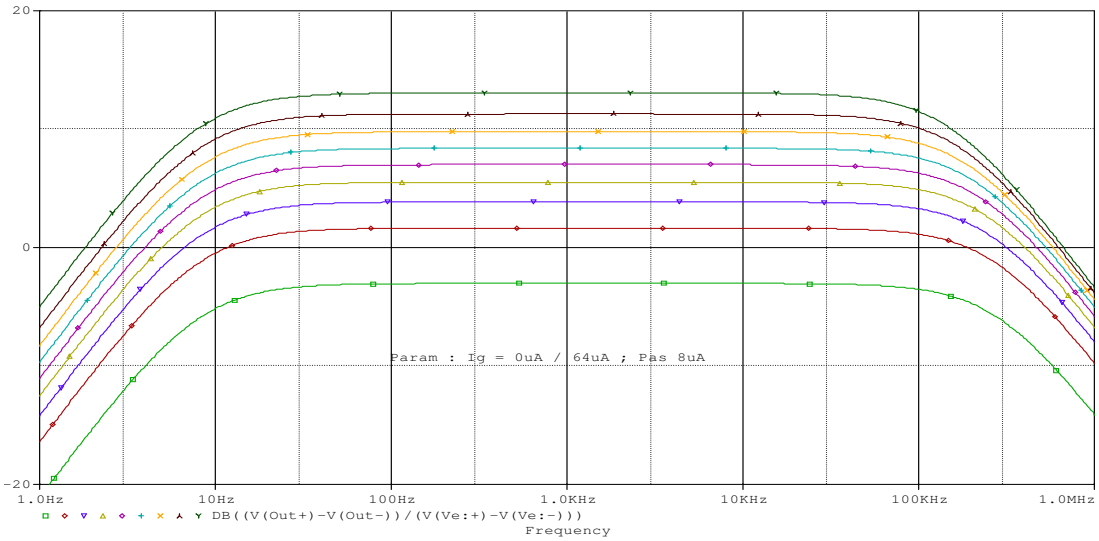

Figure 5. Variation of A_{mg} gain for various I_g values.

Considering this assumption, one could calculate the transistor dimensions of this amplifying A_{mg} module in the next step. Since we would consider low control currents with high dynamics, one should be assured that the transistors operate in high inversion mode ($V_{gs}-V_{TN} \succ 3U_{Th}$). Under these conditions, expression of the drain current could be expressed as follows:

$$I_d=\frac{\beta}{2}(V_{gs}-V_{TN})^2 \text{ ; Or } \quad I_g=\beta(V_{gs}-V_{TN})^2 \qquad (3)$$

Where V_{TN} is the threshold voltage of NMOS transistors and U_{Th} is the thermodynamic potential.

The condition of high inversion mode imposes a limit to us on minimum A_0 gain (Yaïch, 2004):

$$|A_0| \prec \frac{I_0 R}{3U_{Th}} = 0.8 \qquad (4)$$

We would thus take as value $|A_0|=0.5$, which corresponds to $A_{0dB}=-6dB$

Since $|A_0| = g_{m0}R = R\sqrt{\beta I_0}$, we obtain. $\frac{W}{L}=\frac{(\frac{A_0}{R})^2}{K'_n I_0}=1.29$.

For the other transistors corresponding the active load of M_1 and M_2, the same dimensioning could be considered as a first tentative. But in order to maintain a 10KΩ as r_{ds} for each transistor, this dimensioning was tightly modified to 1.25 for the upper one, 1.42 for the middle and 1.65 for the bottom.

The operating point of these transistors M_1 and M_2 (polarised by V_p source) should be also determined among these characteristics of the A_{mg} module (Yaïch et al., 2004): By supposing that the transistors operate in saturation mode ($V_{ds} \succ V_{gs}-V_{TN}$) and that $V_{gs} \leq V_p$ with $V_{TN}=0.515V$, we obtained $V_p \geq 0.82V$. We chose then $V_p=1.1V$, relatively to $\frac{V_{dd}}{3}$, considering V_{dd}=3.2V.

Figure 5 gives AC simulation results of this A_{mg} mod-ule depending on various I_g values :

The simulation results show that, for a given frequency, the gain increases by $A_{0dB}=-3dB$ with $A_{\max dB}=13dB$ when I_g varies from 0 to 64 µA.

A_{mf} Amplification module characteristic

Amf amplification module for controlling the band-width of each filtering structure is also based on one differential amplifier structure produced by two identical transistors M_1 and M_2 (Figure 6). It is a differential pair, with coupled sources that was charged by a current mirror formed by transistors M_3 and M_4. The current source If assured the control of drain currents. Also, by supposing that the transistors (M_1, M_2) as well as (M_3, M_4) are identical, and that $V_{GS1}=V_{GS2}$ and $V_{GS3}=V_{GS4}$, it involves that $I_{d1}=I_{d2}$ and $I_{d3}=I_{d4}$.

In such amplification structure (Yaïch, 2004), by using the equivalent diagram of the MOSFET, the gain variation according to the pulsation could be expressed as follows:

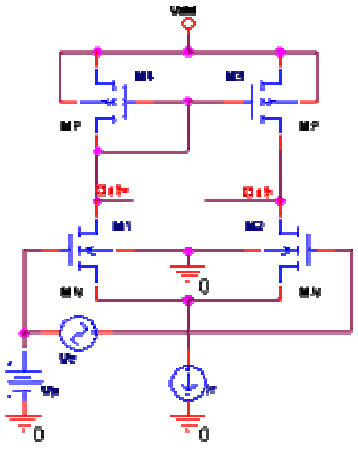

Figure 6. Basic structure of A_{mf} amp-lification structure

$$A_v = \frac{V_{(out-)}}{V_e} = \frac{g_m r_{ds}\left(1+\frac{C_{gs}}{g_m}p\right)}{1+p\left[2r_{ds}C_{gd}+\frac{C_{gd}+2C_{gs}}{g_m}\right]+p^2\left[\frac{2r_{ds}C_{gs}C_{gd}}{g_m}\right]} \quad (5)$$

Considering that $g_m r_{ds}$ represents the gain for medium frequencies having important value (differential amplifier with active load), one could then assume this approxi-mation:

$$2r_{ds}C_{gd} \succ\succ \frac{C_{gd}+2C_{gs}}{g_m}$$

Equation (5) would be then:

$$A_v = \frac{V_{(out-)}}{V_e} = \frac{g_m r_{ds}\left(1+\frac{C_{gs}}{g_m}p\right)}{1+p\left(2r_{ds}C_{gd}\right)+p^2\left(\frac{2r_{ds}C_{gs}C_{gd}}{g_m}\right)} \quad (6)$$

Which would be written as:

$$A_v(\omega)=A_0\frac{1+j\frac{\omega}{\omega_z}}{(1+j\frac{\omega}{\omega_1})(1+j\frac{\omega}{\omega_2})} \quad (7)$$

Where A_0, ω_z , ω_1 and ω_2 are given by:

$$A_0 = g_m r_{ds} \quad (8)$$

$$\omega_z=\frac{g_m}{C_{gs}} \quad (9)$$

$$\omega_1 = \frac{1}{2}\frac{g_m}{C_{gs}}\left[1-\sqrt{1-\frac{2C_{gs}}{g_m r_{ds} C_{gd}}}\right] \approx \frac{1}{2}\frac{g_m}{C_{gs}}\left[1-1+\frac{C_{gs}}{g_m r_{ds} C_{gd}}\right] = \frac{1}{2r_{ds}C_{gd}} \quad (10)$$

$$\omega_2 = \frac{1}{2}\frac{g_m}{C_{gs}}\left[1+\sqrt{1-\frac{2C_{gs}}{g_m r_{ds} C_{gd}}}\right] \approx \frac{1}{2}\frac{g_m}{C_{gs}}\left[1+1-\frac{C_{gs}}{g_m r_{ds} C_{gd}}\right] \approx \frac{g_m}{C_{gs}} \quad (11)$$

Considering that $\omega_2 \approx \frac{g_m}{C_{gs}} = \omega_z$, we could write :

$$A_v(\omega)=A_0\frac{1}{(1+j\frac{\omega}{\omega_1})} \quad (12)$$

with $\omega_1 = \frac{1}{2r_{ds}C_{gd}} = \frac{\lambda_p I_d}{2C_{gd}}$ (13)

where λ_p is the channel length modulation parameter of P transistor and I_d is the drain current.

A_0 could be supposed as constant considering low values of the control current I_f. Then, the cut-off frequency depends on I_d, therefore on I_f since $I_f = 2I_d$.

Bode diagram presents gain characteristic with an adjustable high cut-off frequency. Adjustment could be made on the control current I_f with a slope of 6dB/octave, while having a supposed constant level A_0.

Simulation results of A_{mf} amplification structure, showing the variation of the response for various values of the I_f control current (from 1µA to 41µA with a 10µA step), are illustrated in Figure 6. The transistors dimensions are appropriately selected for $W_n=W_p=100\mu m$ and $L_n=L_p=1\mu m$ (Yaïch, 2004).

We noticed that according to these obtained results, that the first band-widths are high for our audio bands' appli-cation, since the cut-off frequencies varies from 150kHz to 5MHz for the selected control currents. In fact, assuming that the C_{gd} capacitor presents a very low value, and in order to decrease these cut-off frequencies, we added a capacity C_1 around some pF between the grid and the drain of M_3. New expression of the cut-off frequency is given by:

$\omega_1 = \frac{\lambda_p I_d}{2(C_{gd}+C_1)}$; Or $C_1 \succ\succ C_{gd}$, so ω_1 can be approximated by:

$$\omega_1 = \frac{\lambda_p I_d}{2C_1} \quad (14)$$

The results of simulation, given by Figure 7, show that the band-widths were reduced to 470Hz for I_f =1µA and to 15 KHz for I_f = 41µA.

Regarding the low cut-off frequency, such A_{mf} structure does not permit to fix the desired value of this low

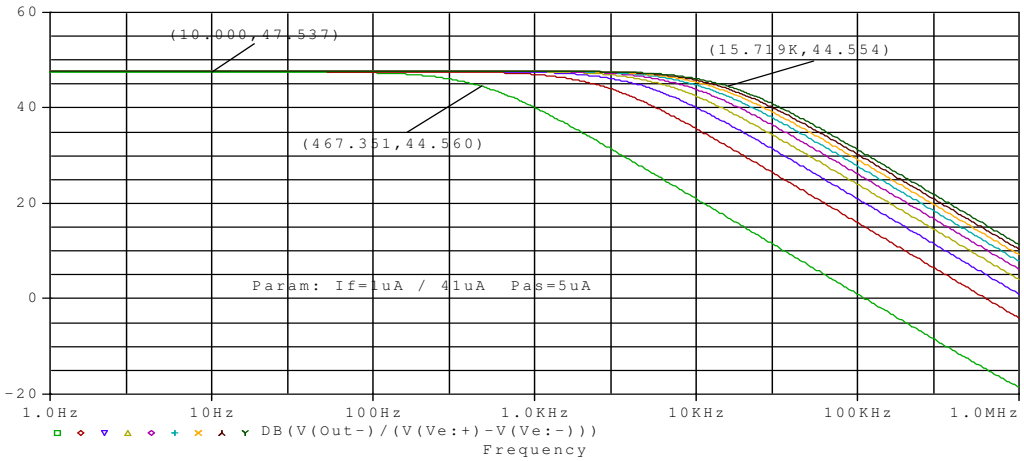

Figure 7: A_{mf} amplification structure: cut-off frequency variation.

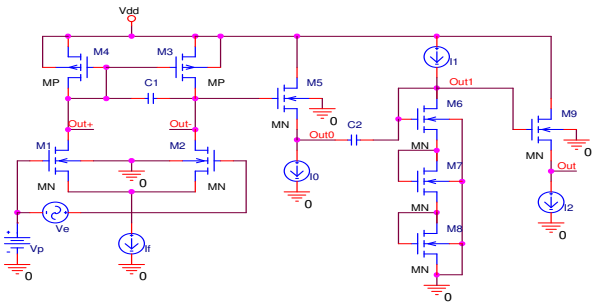

Figure 8: A_{mf} amplification structure: An adjustable band width.

cut-off frequency. We added then, with the preceding structure, an appropriate low pass RC filter associated to an adaptation impedance stage in the output, so to obtain the complete diagram of the following full A_{mf} amplification structure (Ben Amor, 2006) (Figure 8):

As an example for the 5th filter, simulation results give satisfactory values for the desired band width. The values of C_1 and C_2 were fixed to have the desired cut-off frequencies relatively to this considered 5th filter (Figure 9). Results show the effective band-width control using a 6dB/octave slopes. We noted that we shouldn't much reduce the high cut-off frequency in order to conserve the constant desired level A_0.

Digital to Analogue Converter (DAC)

MOS transistor current sources were commanded by a Digital to Analogue Converters 'DAC' assuring then the possibility of programmability of not only the cut off frequencies but also the gain of each structure. In this part, we are interested in the design of one 'DAC' converter, also based on MOS technology to achieve compatibility integration as well as power consumption economy.

Each converter presents a digital input in five bits, a sufficient resolution to control both gain and band-width of the basic amplification stage. Each MOS current source receives then a proportional current relatively to the digital input (D_0, D_1, D_2, D_3, D_4).

The illustrated architecture in Figure 10 (Ghorbel, 2001) permitted the output current generation dependently to a reference voltage Vref. The MOS circuit was composed of five binary balanced current sources carried out with identical P transistors placed in parallel or in series for delivering a programmable current level as : I_0 , $I_1=2I_0$, $I_2=4I_0$, $I_3=8I_0$, $I_4=16I_0$. So, the output current will be then: $I_{out} = D_0I_0+D_1I_1+D_2I_2+D_3 I_3+D_4I_4$.

We simulated the proposed DAC structure by the diagram of Figure 11 using PSPICE software. We choose the BSIM3V3 model of MOS transistors in 0.35µm technology. The switches, represented here by sub-circuits named «COM» (Yaïch et al., 2003), were studied and optimized to avoid the problems of overlapping in the analogical switches (Allen et al., 2002).

The obtained experimental results were confirmed by the theoretical relation (15) with $V_{gs}=V_{réf}-V_{dd}$.

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_T\right)^2 \qquad (15)$$

where C_{ox} is the capacitance per area unit of the gate oxide and µ is the surface mobility of the channel.

From the 'DAC' converter simulation results, we calculated for each branch, the relative error ΔI/I, in order to select the convenient W/L dimensioning (Yaïch et al., 2004) (Table 1). Current variation ΔI was supposed to be

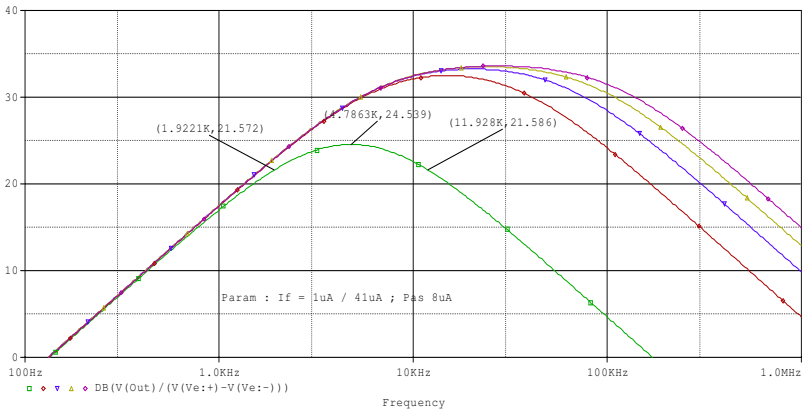

Figure 9. Band pass A_{mf} adjustment.

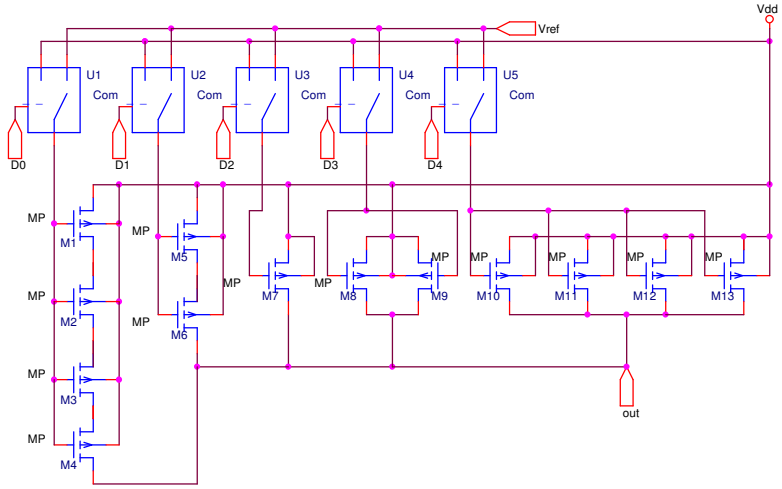

Figure 10. Digital to Analogue Converter 'DAC' simulation circuit .

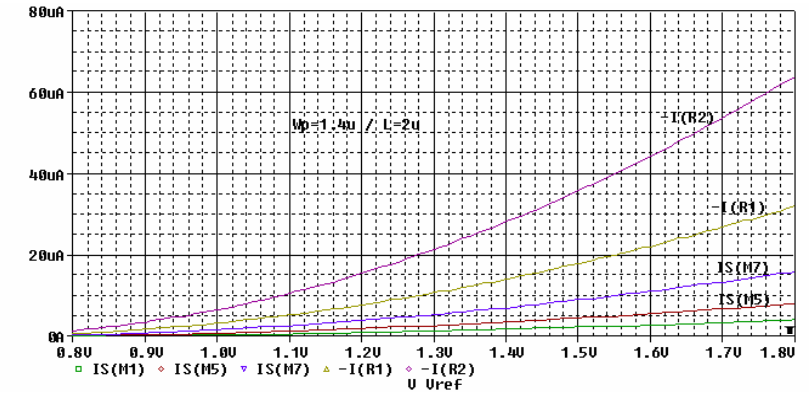

Figure 11. PSPICE 'DAC' converter simulation.

Table 1. Relative current error for different W values

W(µm)	ΔI/I(%); (I4=16I0)	ΔI/I(%); (I3=8I0)	ΔI/I(%); (I2=4I0)	ΔI/I(%); (I1=2I0)	Vref(V)
1	1.15	1.15	1.15	0.2	1.67
1.1	0.58	0.58	0.57	0.8	1.73
1.2	0.13	0.13	0.13	0.17	1.77
1.3	0.27	0.27	0.27	0.33	1.81
1.4	0.7	0.7	0.7	0.5	1.85
1.5	1.05	1.05	1.05	0.62	1.88
1.6	1.33	1.36	1.33	0.73	1.91

Table 2. Recapitulation for the programming control

Data					Decimal value	Current Ig (µA)	Calculated values of Ag Gain (dB)	Measured values of Ag Gain (dB)
D0	D1	D2	D3	D4				
0	0	0	0	0	0	0	-3.00	-3
1	0	0	0	0	1	2	-1.07	-1
0	1	0	0	0	2	4	0.03	0
1	1	0	0	0	3	6	0.95	1
1	0	1	0	0	5	10	2.23	2
0	1	1	0	0	6	12	2.90	3
0	0	0	1	0	8	16	3.90	4
1	1	1	1	0	11	22	5.18	5
1	0	1	1	0	13	26	5.96	6
0	0	0	0	1	16	32	7.05	7
1	1	0	0	1	19	38	8.09	8
0	1	1	0	1	22	44	9.12	9
1	0	0	1	1	25	50	10.19	10
1	1	0	1	1	27	54	10.94	11
0	1	1	1	1	30	60	12.16	12

the difference between simulation value and theoretical value. Minimum ΔI/I error was then obtained for L=2µm and W=1.2µm.

As a recapitulation for the programming control, Table 2 gathers the correspondence between the control current I_g, the $D_0D_1D_2D_3D_4$ five bit command frame of the 'DAC' converter and the relative gain values A selected for A_{mg} amplification module.

With $D_0D_1D_2D_3D_4$ five bit command frame of the 'DAC' converter, I_g control current would be provided as well as its relative A value raging from –3dB to +12dB with a 1dB step. The relative error between the computed values and those measured does not exceed 10%.

Simulation results: Complete filtering structure

One amplification stage: One filtering module

To have more flexibility in handling the various parameters of A_{mg} and A_{mf} modules, these modules were simplified to sub circuits as shown in Figures 12 and 13 (Ben Amor, 2006). Moreover, to avoid any pre polarisation source, we supply our circuits by two voltage sources V_{dd} and V_{ss}.

An improvement of the desired curve response of each filter (12dB/Octave slope) was made by adding capacities C'_h and C'_b in the A_{mg} module as well as in the A_{mf} module. They could then fix the high (F'_h) and low (F'_b) cut-off frequencies respectively (Ben Amor, 2006). Figure 14 shows the final simulation circuit of the first filter. We respectively varied I_f and I_g to adjust the band-width and the gain. Regarding this first filtering module independently, the results of simulation are given by Figure 15. We note then a curve response with 12dB/Octave slope.

Global filtering module

The five filtering modules must be gathered in one global circuit which constituted the hearing aid filtering stage. We must ensure the communication with the external programming system. Capacities C_b, C'_b and C_h, C'_h would be then fixed to the appropriate values in order to maintain best performances (Ben Amor, 2006). The output signals of the filters are converted into current in ord-

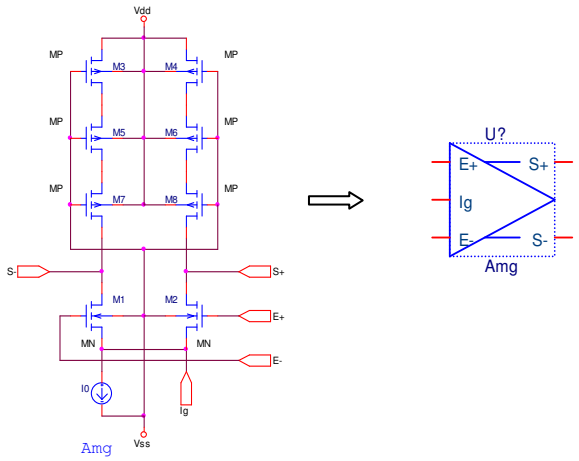

Figure 12. PSPICE A_{mg} sub circuit simulation.

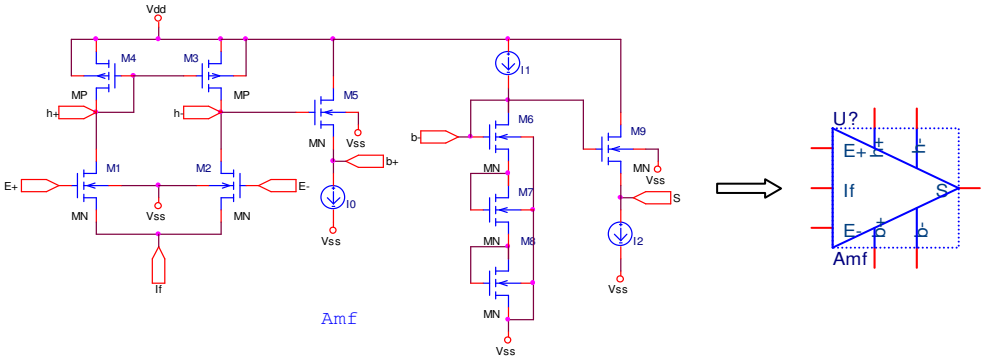

Figure 13. PSPICE A_{mf} sub circuit simulation.

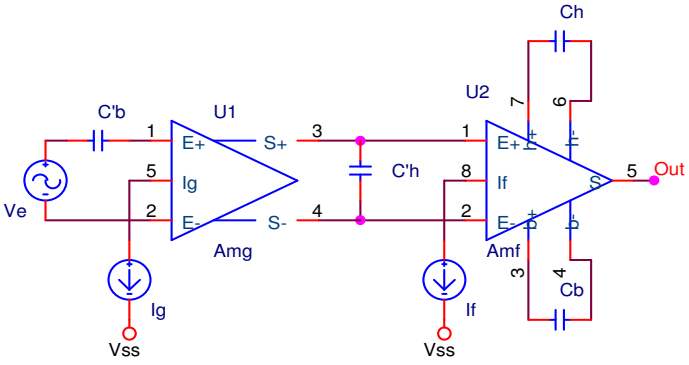

Figure 14. Final circuit of the first filter

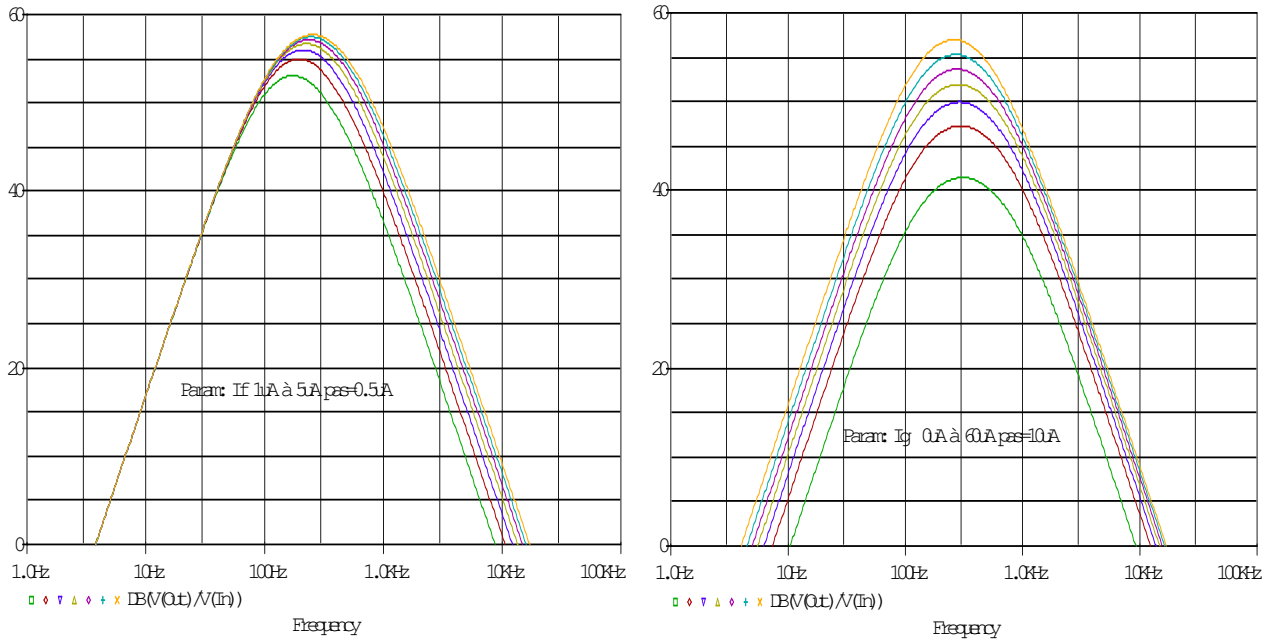

Figure 15. Independent 1st filter simulation: I_f and I_g variation.

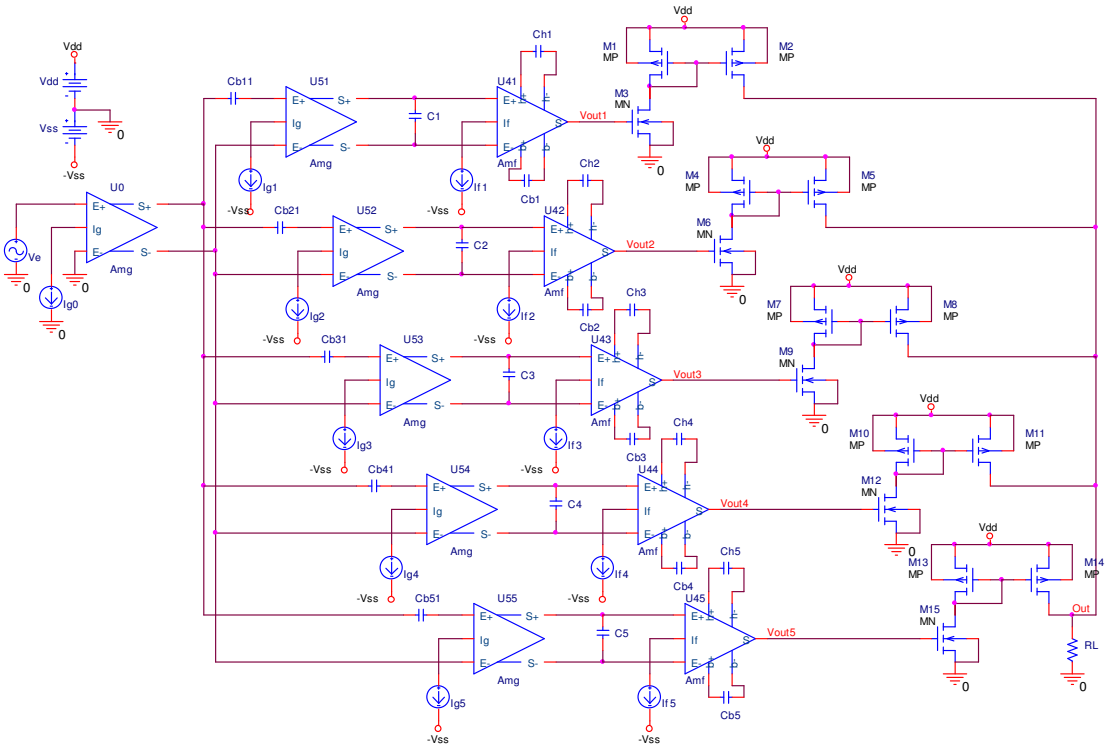

Figure 16. Complete filtering structure: Five filters.

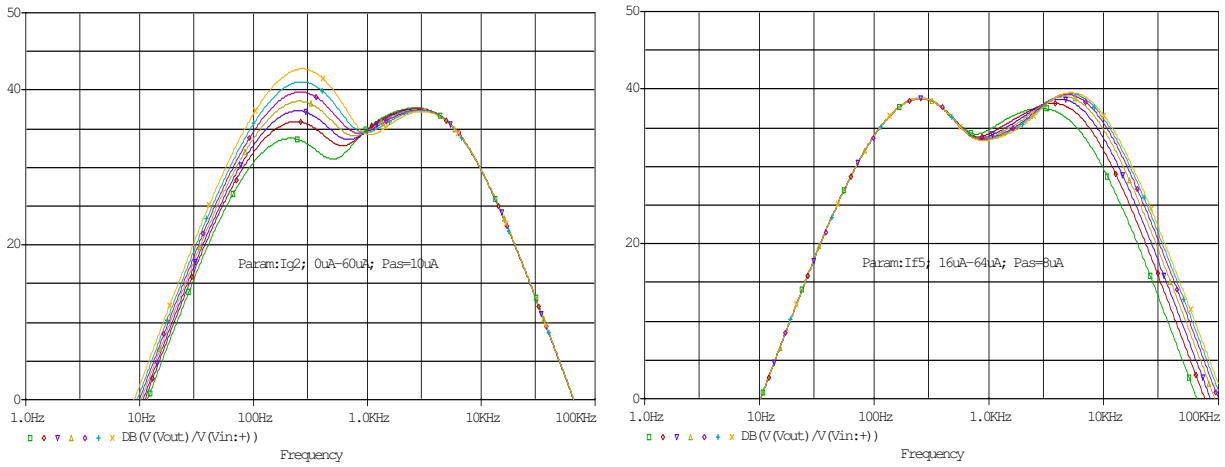

Figure 17. Hearing aid filtering stage simulation: I_g and I_f variation respectively for the 2nd and the 5th filter.

er to be summed (Figure 16), which will give the total response curve of the prosthesis. A pre-amplification stage is added on the input to adapt the input level to the filters.

PSPICE simulation was done for these five filtering modules constituting the hearing aid filtering stage. With Figure 17 the response curve obtained for various values of I_{g2} and I_{f5} was shown demonstrating the then total flexibility in adjusting not only gain value but also band width value. This example shows that it is possible to adjust the parameters I_{gi} and I_{fi} to obtain the form which allows to compensate for hearing deficiency of the patient.

CONCLUSION

We were interested in this paper in the design of a convivial and programmable analogue filtering conception for one hearing aid apparatus. Our design involves an adjustable amplifying chain formed by five analogue but programmable filters. Such filters could be then adjusted according to patient audiogram in order to compensate the considered hearing loss.

Amplifier structure used at each filtering stage was independently controlled using current sources conceived by MOS transistors. At each amplifying structure, one could distinguish two stages referred as A_{mg} and A_{mf}: A_{mg} was conceived to control the filter's gain where A_{mf} was conceived to control frequency band width. On the other hand, these MOS transistor current sources were commanded by Digital to Analogue Converters. The overall circuit was conceived using MOS technology in order to satisfy the low power incessant need for such biomedical applications.

This design concerned flexibility, performance as well as efficiency regarding different programmable parameter. Indeed, all digital information will be sent from a PC to be then stored on an EPROM contained on the apparatus. Flexibility and best performances in this biomedical apparatus could be an efficient reason for exploring total hearing capacities of patients and satisfying different pathological cases' needs.

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