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Full Length Research Paper

Design and analysis of 45 nm low power 32 kb embedded static random access memory (SRAM) cell

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In sub-100 nm generation, gate-tunneling leakage current increases and dominates the total standby leakage current of LSIs based on decreasing gate-oxide thickness. Showing that the gate leakage current is effectively reduced by lowering the gate voltage, we propose a local DC level control (LDLC) for static random access memory (SRAM) cell arrays and an automatic gate leakage suppression driver (AGLSD) for peripheral circuits. We designed and analyzed a 32 kb 1-port SRAM using 45 nm CMOS technology. The six-transistor SRAM cell size is 1.25 μm^2. Evaluation shows that the standby current of 32 kb SRAM is 1.2 μA at 1.2 V and room temperature. It was reduced to 7.5% of the conventional SRAM.

Key words: Embedded static random access memory (SRAM), gate leakage, low power, standby current, random access memory (RAM).

INTRODUCTION

In accordance with rapid development micro fabrication technology, the effect of gate leakage current becomes dominant in the standby mode of systems-on-chip (SoC). This is mainly because thinner gate-oxide film increases the probability of quantum tunneling between the poly gate and the inversion layer (Agarwal et al., 2003; Bhavnagarwala et al., 2003). Especially in 45 nm complementary metal oxide semiconductor (CMOS) technology nodes, we cannot neglect the gate leakage current originating from an embedded static random access memory (SRAM) which occupies most of the area in SoC. Therefore, in order to apply some CMOS devices fabricated in 45 nm technology nodes to various mobile applications, we have to enlarge the gate-oxide thickness to realize very low standby power. The power supply voltage, however, is scaled down based on the scaling law; the drain current decreases if the gate-oxide thickness is not scaled down. This keeps us from achieving high-speed operation and from realizing the scaling merits. To solve such problems, several methods have been proposed. For example, it was reported that the thin gate oxide was applied only to the critical path by dual or triple gate oxide technology (Bhavnagarwala et al., 2001). However, because of the difficulty in controlling the gate-oxide thickness locally, this method is not feasible. On the other hand, high-material, which is considered to be an alternative to conventional SiO_2, has attracted much attention in research (Chandrakasan et al., 2000). Making use of the high-materials, it is possible to suppress the gate leakage current, because the physical thickness of the high-material is larger than that of the conventional SiO_2 film of the same dielectric constant. Even if the high-material is used in the gate oxide, however, one will encounter the same problem as SiO_2 film, namely, that the gate leakage current cannot be neglected in future device scaling. In other words, the quantum mechanical behavior inevitably makes an appearance through the scaling of the high insulation film.

Therefore, the problem of the gate leakage current which appears in 45 nm technology nodes will become more serious in future CMOS devices. In this paper, to suppress the gate leakage current without complicated fabrication processes, we propose new design method for an embedded SRAM using our original circuitry.

This paper is organized as follows. The relation between gate voltage and gate leakage current was quantitatively discuss. Showing that to lower NMOS gate voltage is the most crucial factor to suppress the total gate leakage current, how we perform this gate voltage lowering method both in the memory cell array and in peripheral

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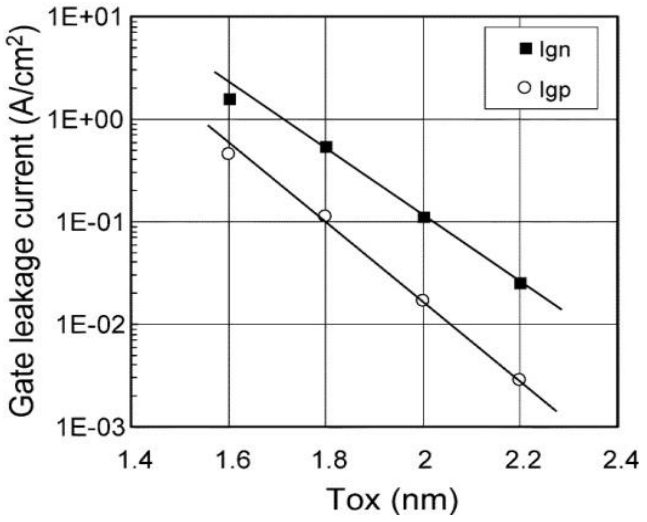

Figure 1. Gate leakage current versus T.

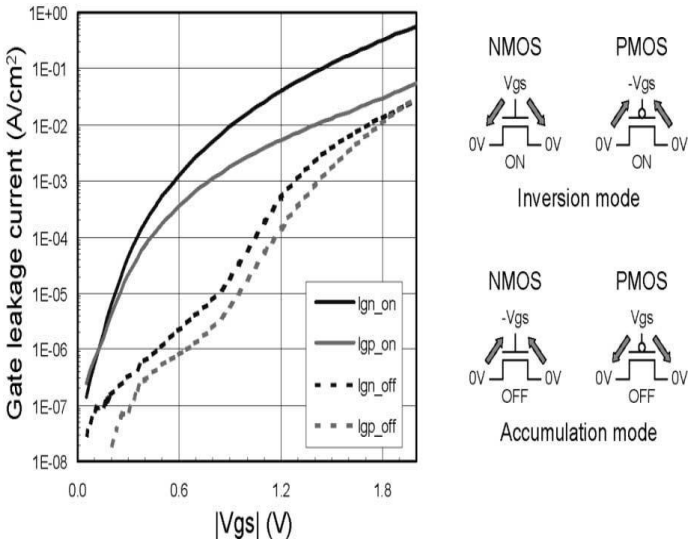

Figure 2. Gate leakage current versus gate voltage (EOT = 2:0 nm).

circuits was explained. The detailed structure of our test chip In Section IV was shown. A 32-kb SRAM is fabricated by means of 45 nm CMOS logic process. Finally, the standby leakage current was evaluated and showed that it is suppressed as compared to the conventional embedded SRAM, and a brief summary was given.

GATE LEAKAGE ISSUE

In recent microprocessors, the capacity of on-chip memory is rapidly increasing to improve overall performance. According to the International Technology Roadmap for Semiconductors (ITRS) road map in 2001 (Enomoto, 2003), memory will occupy about 45% of chip area in 2013. In such a memory-rich chip, the leakage current of an embedded SRAM dominates the standby current. Thus, the reduction of the standby leakage current of SRAMs is the most important factor to achieve low power consumption.

When supply voltage is scaled down, the sub threshold leakage current, which is one of the main contributors to the standby leakage in SRAM, tends to increase due to decreased threshold voltage (V_{th}) of the transistors. A dual V_{th} technique is generally used to reduce the sub threshold leakage current in a system large scale integration (LSI). Using low-(high) V_{th} transistors in the critical (noncritical) path, one can improve both speed and power. This dual V_{th} technique is easier than the multi-gate-oxide technique mentioned earlier, so that the sub threshold leakage current can be reduced by optimizing V_{th}.

Figure 1 shows the relation between the gate leakage current and the thickness of the gate insulation film. The vertical axis shows the gate leakage current per unit gate area, and the horizontal axis shows the physical oxide thickness of the gate insulation film. The gate leakage current increases exponentially as the physical thickness of gate insulation film become thinner in keeping with scaling. The gate leakage current of NMOS is 4 to 10 times greater than that of P-type metal oxide semiconductor (PMOS) of the same thickness.

Figure 2 shows the relation between the measured gate tunneling current of the MOS transistor and gate voltage in our 45 nm CMOS logic technology (Imai et al., 2000). The equivalent gate-oxide thickness is 2.0 nm. Note that there are two types of modes in the direction of gate leakage currents: one is inversion mode, in which the leakage flows in the turned-on MOSFET, and the other is accumulation mode, in which it flows in the turned-off MOSFET. The directions of the gate leakage currents are also depicted on the right side of Figure 2. Because of the difference of this leakage direction, dependence of the gate leakage current differs from the inversion mode and the accumulation mode, as shown in Figure 2. At an operating voltage of 1.2 V, the inversion current of N-type metal oxide semiconductor (NMOS) is the largest in all modes. Furthermore, when the gate voltage is changed from 1.2 to 0.6 V, the gate leakage current is suppressed to about 1/10 of the leakage current at 1.2 V. Therefore, lowering the NMOS gate voltage reduces the gate leakage current in LSIs. Subsequently, according to the aforementioned consideration, we propose a method to suppress the gate leakage current for an embedded SRAM.

SUPPRESSING GATE LEAKAGE CURRENT IN SRAM

Having found the effectiveness of lowering the NMOS gate voltage, we now show how we introduce this characteristic feature to our circuitry. In this study, we employ two ways to reduce the gate leakage current: one

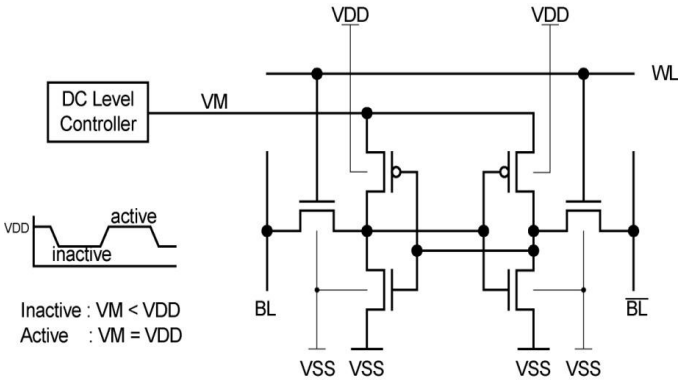

Figure 3. Leakage model in six-transistor SRAM cell.

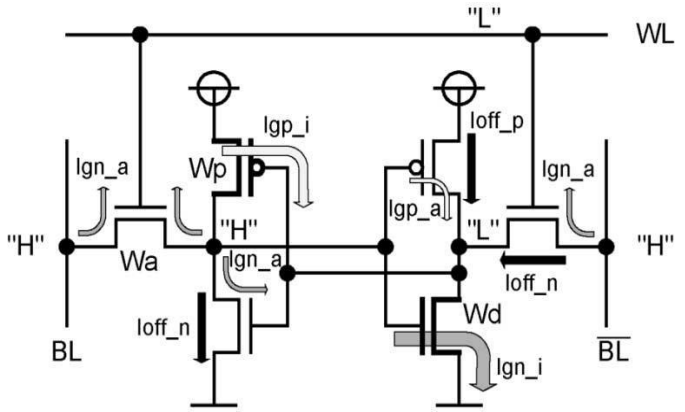

Figure 4. Gate leakage current suppression in a cell.

is to control the power supply voltage of the memory cell dynamically, and the other is to modify the conventional peripheral circuit.

Memory cell

Figure 3 shows the leakage model in a six-transistor (6T) SRAM cell. When the cell is inactive, the word line (WL) is low level (“L”) and bit lines (BL), are high level (“H”). One storage node of the cell is “H” and the other is “L.” Then, the gate leakage current I_{gcell} and drain leakage current $I_{off\ cell}$ of a cell are calculated as follows:

$$I_{g\text{-}}cell = W_p.I_{gp\text{-}I} + W_p.I_{gp\text{-}a} + W_g.I_{gn\text{-}I} + (W_d + 3\,W_a)I_{gn\text{-}I} \quad (1)$$

$$I_{off\text{-}}cell = W_{p.}\,I_{offp} + (W_d + W_a).\,I_{offn} \quad (2)$$

where W_a, W_d, and W_p are the gate widths of the access transistor, driver transistor and load transistor, respectively. I_{offp} (I_{offn}) represents the drain leakage current per unit width for PMOS (NMOS). $I_{gp\text{-}}i$ ($I_{gp\text{-}}i$) and $I_{gp\text{-}}a$ are the gate leakage currents of unit width in the inversion mode and the accumulation mode, respectively. The standby leakage current of a memory cell can be estimated by the sum of $I_{g\text{-}}$cell and $I_{off\text{-}}$cell, here, gate-induced drain leakage (GIDL) is ignored because it is smaller than 1/10 of the total drain leakage current in our 45 nm CMOS technology (Imai et al., 2000). Since the inversion current of NMOS is dominant in gate leakage currents (Figure 2), the third term in (1) is the most dominant factor. Therefore, we focus on the suppression of the gate leakage current of the NMOS driver transistors.

Here, we adopt the method to control the potential of the source line of the memory cells in order to reduce the gate leakage current in an inactive mode. Figure 4 shows the basic concept of this method. Node VM (PMOS source line) is disconnected from the PMOS substrate lines connected to the supply voltage. The NMOS source line is commonly connected to ground line with NMOS substrate lines. A DC level controller is introduced to control the VM potential dynamically. By means of this circuitry, the VM potential is lowered during inactive mode, which leads to the lowering of the gate voltage of the driver transistor.

Before developing our discussion, we have to comment on the merit of lowering VM potential. Various methods of controlling source line potential to reduce leakage current have been reported so far (International Technology Roadmap for semiconductors, 2001; Matsumoto et al., 2003; Nii et al., 1998; Oh et al., 2003; Osada et al., 2001, 2003; Sze, 1981). Lowering the V_{DD} source line has the advantage of reducing the sub threshold leakage current of the PMOS load transistor. This is due to a reverse body bias effect of the PMOS originating from the decrease of the source voltage. In addition, because of the enhancement of drain-induced barrier lowering (DIBL), the sub threshold leakage current in both the NMOS driver transistor and the PMOS load transistor are reduced. Note that this method does not address the sub threshold leakage current in NMOS access transistors. In particular, as for the access transistor between the precharged bit line and the cell node stored “H” the sub threshold leakage current might slightly increase. However, compared to the sub threshold leakage of the access transistor in the opposite side, this leakage is so small that we can ignore it. On the other hand, it is well known that raising the GND line is also an effective way to reduce the sub threshold leakage current of the access transistor and the driver transistor. This is mainly responsible for the substrate bias effect of NMOS. In this method, the DIBL reduces all the sub threshold leakage current in both NMOS and PMOS.

As for the reduction of the gate leakage current in the SRAM cell, both methods mentioned earlier are effective. Lowering the V_{dd} source or raising the GND source can decrease the gate-source voltage of the NMOS driver transistor, which results in the large reduction of total gate leakage current. Therefore, it is important to choose the appropriate method to suppress the most dominant leakage current effectively. In this study, we only treated

Table 1. Target specifications of leakage for 45 nm low-power CMOS technology.

Leakage specification (pA/µm)		R.T		40°C	
		Typ. process	Leakage worst	Typ. process	Leakage worst
I_{off}	NMOS	4	16 (×4)	R.T. × 2	
	PMOS	4	16 (×4)		
I_g	NMOS (inv)	40	200 (×5)	R.T. ×1	
	PMOS (inv)	5	25 (×5)		
	NMOS (Acc.)	<1	<3 (×3)		
	PMOS (Acc.)	<1	<3 (×3)		

Table 2. Transistor sizes of 6T SRAM cell.

Cell dimension	Width (nm)	Length (nm)
Acess Tr.	140	
Driver Tr.	200	45
Load Tr.	140	

Table 3. Standby leakage current of 6T SRAM cell.

Condition		I_{off} (pA)	I_g (pA)	Total (pA)	I_g/Total (%)
R.T.	Typical	1.92	9.46	11.38	83.1
	Worst	7.68	45.78	53.46	85.6
40°C	Typical	3.84	9.46	13.30	71.1
	Worst	15.36	45.78	61.14	74.9

the lowering of the V_{DD}, because the gate leakage current is the most dominant factor in our 45 nm CMOS process, as shown in Table 1. The gate leakage current in NMOS (Inv.) is one order of magnitude larger than others, so that the total standby current can be reduced effectively by lowering. In addition, to suppress the extraordinary leakage caused by some fail bits, it is convenient to cut the power supply line of the corresponding cell block for repair. Another reason to use V_{DD} control is that it is easier to handle the V_{dd} line from the viewpoint of layout design. Moreover, in the case that the GND source line is controlled, it might cause undesirable access delay due to the additional pull-down NMOS switch. Otherwise, in the case of controlling the source line, the pull-up PMOS switch does not affect the access time because there are no cell current flows in it.

By means of the process data in our 45 nm CMOS technology, we can estimate the leakage current of a 6T SRAM cell. The target specifications of the leakage current are summarized in Table 1. Here, I_{off} is the drain current of the turned-off MOSFET, which includes GIDL and sub threshold leakage current. As mentioned earlier, GIDL is negligible in our process, so that the I_{off} is equal to sub threshold leakage current in any process condition and moderate temperature for mobile applications. Substituting the transistor dimensions of the 6T SRAM cell (Table 2) and leakage specifications to Equations 1 and 2, we can obtain the leakage current of a unit cell. The estimations of leakage current are as shown in Table 3. It becomes 11.4 pA at room temperature in the typical process, and 61.1 pA at 40°C in the leakage-worst process, respectively. It was found out that the gate leakage current accounts for a large percentage of the total standby current of the cell.

Figure 5 represents the standby leakage current at VM = 1.2 V for various combinations of process type (Typ. and Leakage-worst) and temperature (R.T. and 40°C). In addition, the standby leakage currents with lowered VM potential (VM = 0.6 V) are also shown. Note that the gate leakage current I_g dominates the largest part of the total standby leakage at VM = 1.2 V. From these results, the gate leakage current was reduced to about 1/10 by lowering VM potential. Moreover, owing to the effect of back gate bias in the PMOS and that of DIBL, this reduced to a half approximately. As a result, it was found out that more than 80% reduction of the total leakage current of memory cell was achieved in inactive mode by lowering the V_{DD} source line. During the active period, in which theSRAM is in read or write operation mode, the VM potential is set to V_{DD}, resulting in the increase of the gate leakage current. However, since the power in read or write operation is mostly consumed in charging and discharging bit lines, increase in the gate leakage current in the active cell does not affect overall active power.

Moreover, to maintain performance and ensure cell stability, the VM potential must be recovered to even if the gate leakage current is increased. Figure 6 shows the measured DC characteristic of 6T SRAM cells in the 45 nm CMOS process. The measured static noise margin is sufficient for stable read-out operation (Tomita et al., 2002).

Peripheral circuit

Here, we deal with the reduction of the gate leakage current in the peripheral circuit. In the peripheral circuit, most gate leakage current flows in the WL driver circuit of a row decoder. Figure 7a shows the conventional WL driver circuit. The largest NMOS transistors in the final stages are turned on to drive the word lines to low level,

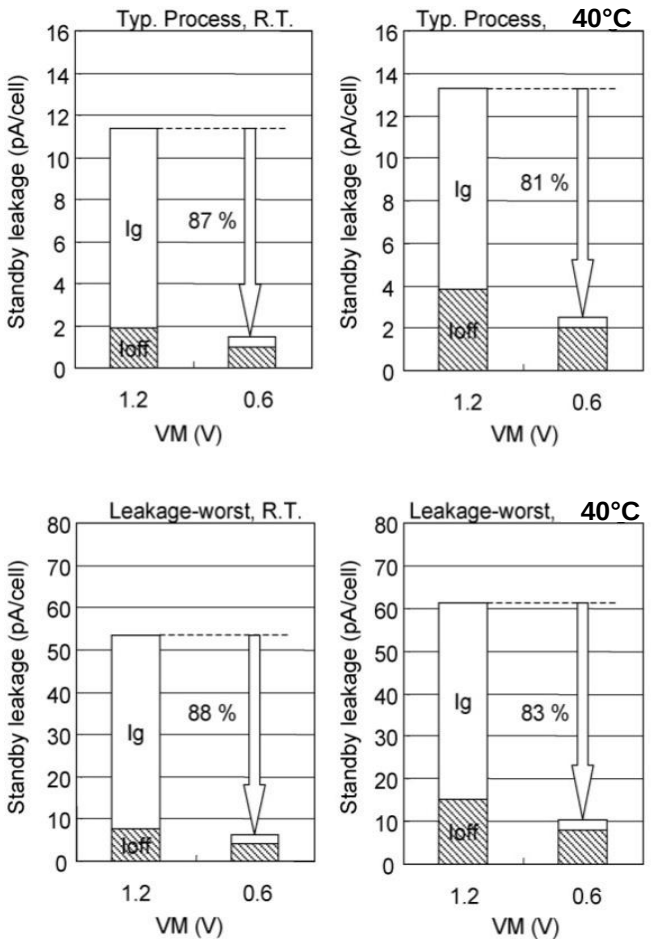

Figure 5. Effect of leakage reduction of 6T SRAM cell.

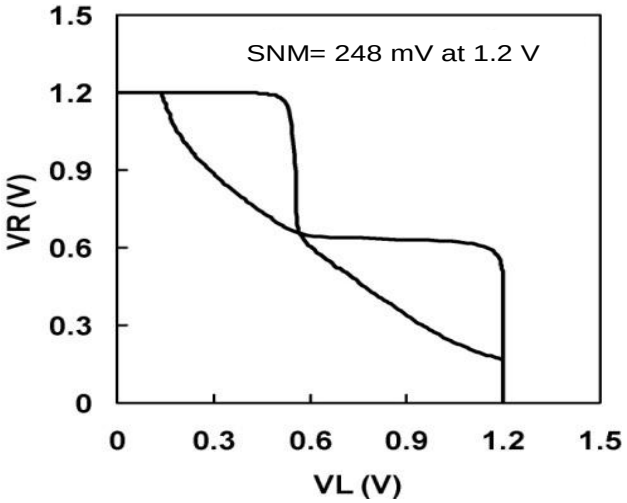

Figure 6. Static noise margin (SNM) of 6T SRAM cell.

except for one accessed row. As shown in the relation between gate voltage and gate leakage current, the gate leakage current of NMOS turned on is dominant. In order to estimate the contribution of the peripheral circuit to the total standby leakage current per unit row, let us compare the gate leakage current of one row and that of the largest NMOS in the WL driver. From Equation 1, the gate leakage current of the memory cells in one row is approximately represented as $I_{g\_}row = W_d . I_{gn\_}i.N$, where N is the number of the total columns of memory cell array. On the other hand, the gate leakage current of the final stage NMOS in the WL driver (W_{d1}) is the gate width which can be expressed as $I_{g\_}peri = W_{d1} . I_{gn\_}i$. If we assume that N = 256 and W_{d1} = 5 µm, the gate leakage current of cells and a WL driver in unit row become 2048 and 200 pA, respectively. This indicates that by controlling VM voltage to reduce the leakage current in the memory cell, the leakage current in the peripheral circuit becomes almost the same as that in the memory cell array. Therefore, we also reduce the leakage current originating from the WL driver.

Figure 7b and c shows the new WL driver to suppress the gate leakage current. We call it an automatic gate leakage suppression driver (AGLSD). Figure 7b shows the schematic diagram and Figure 7c, the timing diagram. Symbols XL, XM and XH denote decode signals. Transistors Qp1 and Qn1 drive the WL. Gate inputs Qp1 and Qn1 are separated from each other in internal nodes i_p and i_n , which are connected via PMOS pass transistor Qp2. The gate of Qp2 is controlled by the WL. When the WL is selected, both i_p and i_n become “L.” The activated WL is charged by Qp1. After a read or write operation is completed, nodes i_p and i_n are set to “H.” The WL is discharged by Qn1. Then, the gate node of Qp2 becomes “H”. Therefore, the node becomes floating because Qp2 is turned off. As the large gate leakage current of Qn1 gradually decreases, the potential of node i_n, the Qn1 gate leakage current itself rapidly decreases. As a result, Qn1 is turned off. This is how the gate leakage current in Qn1 is eliminated. The small NMOS Qn2 keeps the WL to “L” after the Qn1 is turned off. In this way, we can reduce the gate leakage current in peripheral circuits. The gate leakage current of Qn2 is negligible, because its gate width is much smaller than that of Qn1.

DESIGN OF 32 kb 1–PORT SRAM

Here, we detail the proposed local DC level control that dynamically controls VM source lines in the cell array. Figure 8 shows the schematic diagram of the local DC level controller (LDLC). The LDLC controls one VM line which shares the source line of one cell block. Moreover, the VM line is connected to four PMOS pull-up transistors (Q1 to Q4). The Q3 is connected with the V_{DD} through the single-stacked diode. The Q4 is connected with the V_{DD} through the double-stacked diodes. The Q1 and Q2 of the remainder are directly connected with V_{DD}. The DCL0, DCL1 and DCL2 signals play a role which changes the VM potential lowering in the inactive mode.

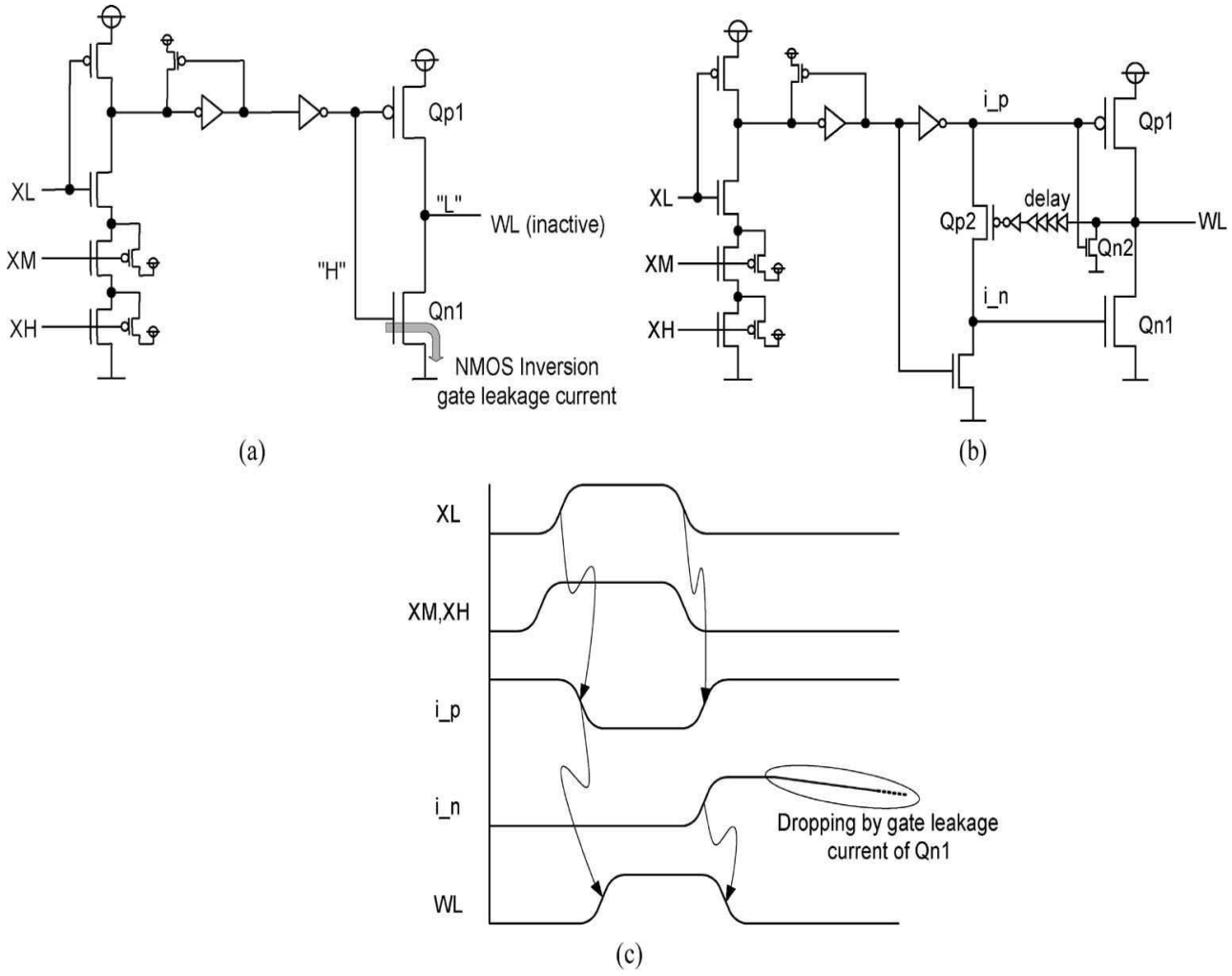

Figure 7. Word line driver circuit with I suppression. (a) Conventional (b) Proposed (c) Timing waveform.

A block enable signal (BS) is introduced to select the cell block in case it contains the addressed memory cell for read or write operation. A KILL signal is introduced not to select the cell block in case it contains some failed bits. This failed block is replaced to the spare block by a repair circuit and the power supply of this failed block is cutoff to reduce extraordinary leakage current. When the BS signal is set to "H" (activated cell block), the PMOS transistor Q1 pulls up the VM potential to V_{DD}. On the other hand, when the BS signal is set to "L" (in activated cell block), the VM potential is controlled by turning on one of Q2 to Q4. If DCL2 signal is "L, the VM potential becomes V_{DD}-2V_{tp}, where V_{tp} is the PMOS transistor threshold voltage. If DCL1 signal is "L," the VM potential becomes V_{DD}-V_{tp}. Therefore, the VM potential has one of the three levels V_{DD}, V_{DD}-V_{tp} and V_{DD}-2V_{tp}, depending on the DCL0, DCL1 and DCL2 signals. By means of this circuitry, we can select the optimum level based on the supply voltage. This is how the lower VM during inactive mode is achieved. The potentials of the VM source line are summarized in Table 4.

Based on the aforementioned preparations, we constructed a 32 kb 1-port SRAM (Figure 9). LDLC is located at the center of each cell block, which consists of 4 columns and 64 rows. The VM lines of the selected cell blocks rise to V_{DD} via corresponding LDLC circuits. Note that, in our method, the VM potential of the addressed cell block should be raised to Vdd level before the corresponding WL is activated. To achieve this functionality, the block-enable signals BS0–7 are connected to the upper predecode signal (XH) which transfers signal faster than the other predecode signals (XM and XL). After WL is deactivated, the VM potential is lowered to V_{DD}-2V_{tp} by its leakage current for a long cycle. If the same cell block is consecutively activated at the next cycle, the VM potential almost keeps V_{DD} level, so that the extra power for charging up the VM is not consumed. In standby mode, no cell block is activated for a long time, so that all VM lines are lowered to V_{DD}-V_{tp}, V_{DD}-2V_{tp}. In the peripheral circuit, we use the WL driver (AGLSD) proposed in the previously. This is how the gate leakage current of SRAM macro was suppressed

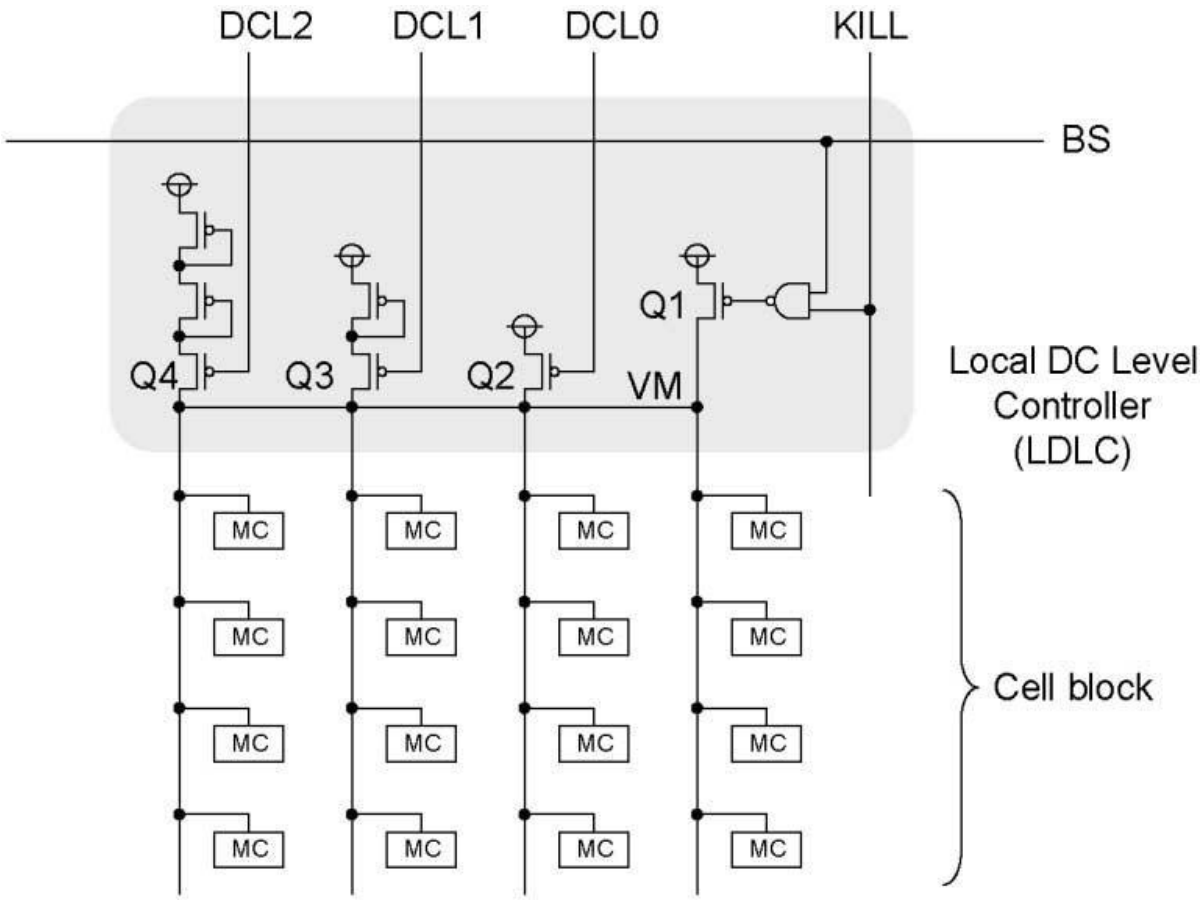

Figure 8. Schematic diagram of LDLC.

Table 4. Status of cell block.

BS	KILL	DCL0	DCL1	DCL2	VM potential	Status of cell block
		H	H	L	V_{DD}	
L		H	L	H	V_{DD}-V_{tp}	Inactivated
	H	L	H	H	V_{DD}-$2V_{tp}$	
H		X	X	X	V_{DD}	Activated
X	L	H	H	H	Hi-Z	Replaced and cutoff the power

dynamically. Figure 10 shows simulated waveforms in read operation especially when the memory block is switched from inactive to active. In this simulation, we assume that DCL2 is selected as shown in Table 4. In inactive mode, the VM line voltage is set to (V_{DD}-$2V_{tp}$) of 0.62 V for 1.2 V supply voltage. From this waveform, it is confirmed that the VM line rises to 1.2 V before the corresponding WL is activated. Accordingly, the cell current and static noise margin are guaranteed. The simulation showed that 32 kb SRAM access time is 2.3 ns at 1.2 V and room temperature.

Conclusion

We have proposed a technique for suppressing gate leakage current for embedded SRAM in SoC. In order to reduce the gate leakage current in a cell array, we have adopted the LDLC circuit which controls the potential of the source line of the memory cells dynamically. We have also proposed the AGLSD circuit which can reduce gate leakage current in the peripheral circuit. We have successfully designed and analyzed a 32 kb SRAM using 45 nm CMOS technology. Test results show that standby

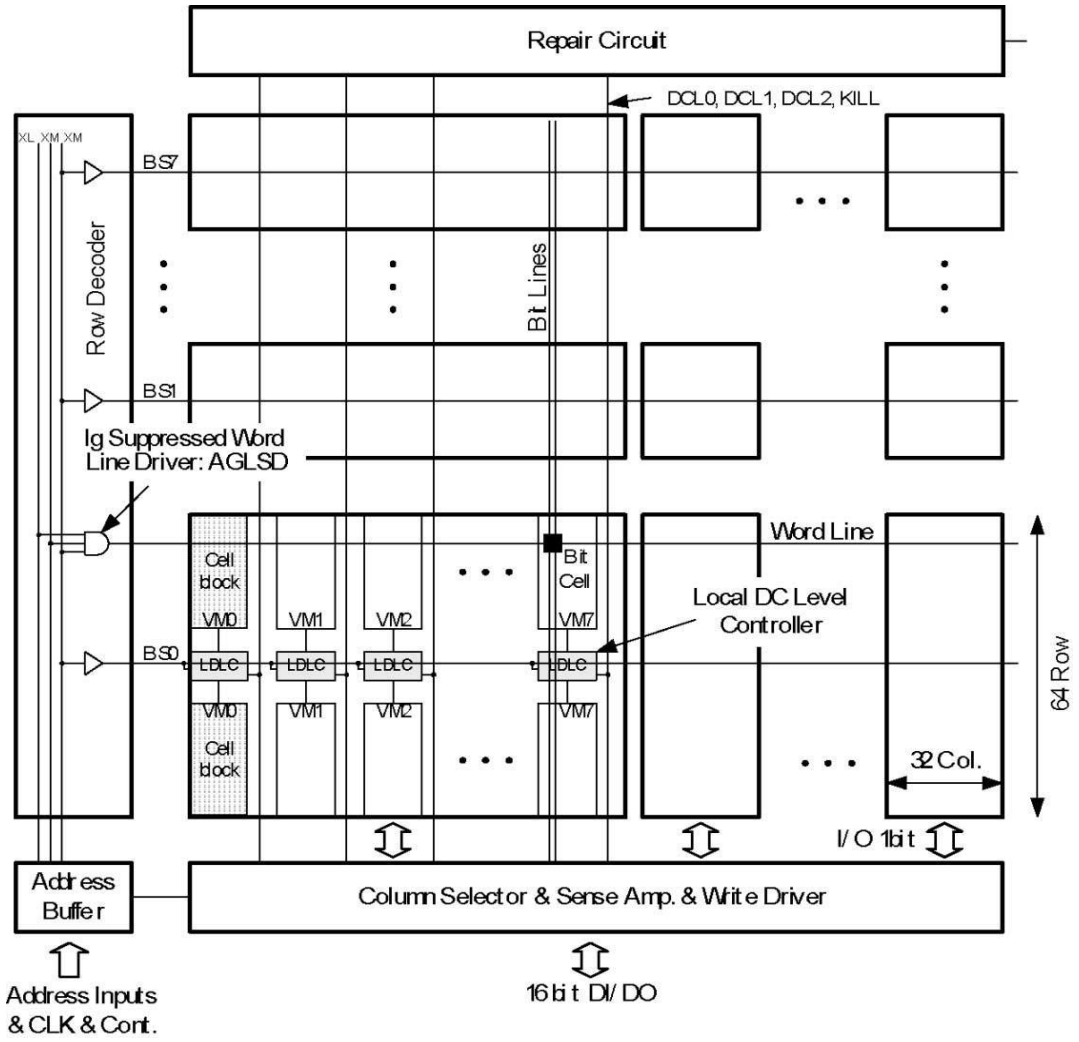

Figure 9. Schematic diagram of 32 kb SRAM with I_g suppression.

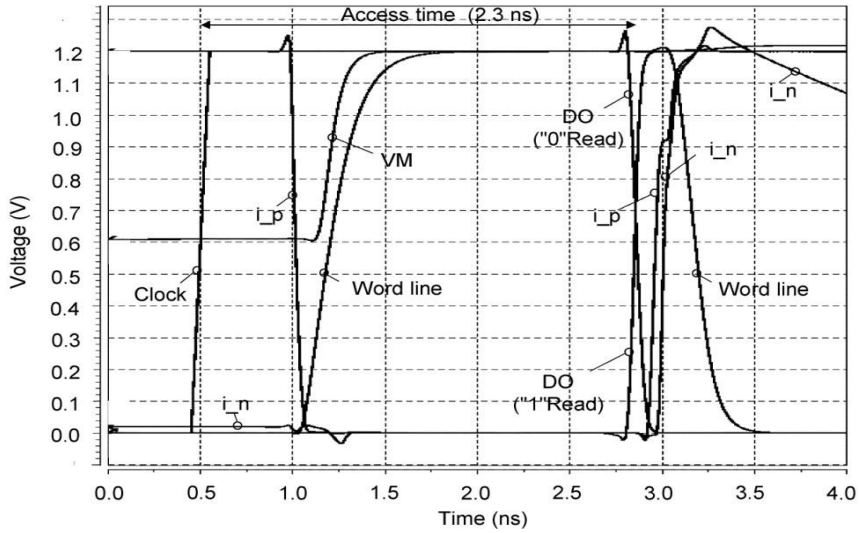

Figure 10. Simulated waveform in read operation.

leakage current was reduced to 7.5% of a conventional SRAM without speed penalty. This will help to realize high-performance ultra-low-power SoCs for mobile applications.

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