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Full Length Research Paper

Design and synthesis of FPGA for speed control of induction motor

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The industrial motor control is quickly changing from micro to nanotechnology design with speed and performance based design implementation. Considering accuracy and synchronism of output response, the attention has been brought to fully digitized design to adopt Space Vector Pulse Width Modulation (SVPWM) as a control technique for three phase Induction Motors due to its resulted advantages in harmonic reduction. Very High Speed Hardware Description Language (VHDL) digitized scheme built on the platform of a Field Programmable Gate Array (FPGA) for direct speed control of Induction Motor has been proposed for industrial applications. This paper proposed hybrid hardware model of analog, digital, power and micro-electronics. The model is focused to industrial application with loss minimization and smooth control of flux. Xilinx 8.1i, Spartan-II FPGA Xc2s50-5pq208, IGBT CT60AM18F, 2HP Induction Motor has been used for design and synthesis of model. The result shows 74% occupied slices and 70% total no of 4 look-up-tables (LUTs) have been utilized. The model response has been observed very smooth.

Key words: Field Programmable Gate Array (FPGA), look-up-tables (LUTs), Space Vector Pulse Width Modulation (SVPWM), Very High Speed Hardware Description Language (VHDL).

INTRODUCTION

Modern industrial motor control units include many micro-controllers and digital signal processors (DSP) interface. The number of varieties, adopted schemes and devices are advancing rapidly. Motor controllers are generally implemented using PID (Proportional Integrated and Derivative) algorithms (Changuel et al., 1996). The voltage/ frequency (V/f) control of induction motor is mostly studied in this regard because of the reason that switching power converters can regulate voltage, current and frequency (Richard et al., 2006). Switching power converters are also suitable to control critically high transient response of voltage and current applied at motor to achieve faster dynamic response. With the improvement in faster dynamic control and its signal processing the need of new high speed processor has increased to be adopted by power semiconductor devices. In today's industrial scenario the ac motors (induction/universal/servo etc.) are digitally controlled through microprocessors/ microcontrollers/ Digital Signal Processing (DSP) modules by PWM techniques.

The advantage can only be attained when it is interfaced with analog circuitry. This has provided many advantages like smooth loss-less control, less generated noise, harmonic reduction, easy control of transient etc. but it is suffered by major disadvantages like complexity in its circuits, restricted function, no circuit modification, application and component specific. In the recent past the modification in VLSI (Very Large Scale Integration) designing has revolutionized the possibility of embedded

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systems to be software adopted computer based control of such industrial applications. The hardware description lan-guage (HDL) has approached the development of modern electronic products to be more application specific integrated circuits (ASIC). It has the possibility to implement the application specific algorithms with the use of its library functions, which is in many ways a low-cost manufacturing and optimal design solution.

The Field Programmable Gate Array (FPGA) is one of the substitutes to the major disadvantages of the conventional microprocessors/DSP control, due to its one major advantage that it can be modified to perform any application and is not specific to a particular function (Ying-Yu-Tzou and Hau-Jean, 1997). The FPGA has on field control/ re-programmable/ convenient software tool/ high efficiency /very high significant integration density (Richard et al., 2006). In this paper we try to emulate the design and implementation of FPGA based motor control and how efficiently they are when it comes to yielding low power norms. A flow diagram based on VHDL as shown in Figure 1 is the basis of implementation.

HARDWARE IMPLEMENTATION

Experimental setup

Constant volts per Hertz (V/f) mode of operation for Induction Motor is an old method and very well acceptable for low range (even less then 1 Hz) of speed control. Ideally it is notified that torque-speed charac-teristics can be reproduced at all frequencies. If inverter nonlinearities have not been compensated adequately then they may cause distortion output voltages, pulsating torques leading to vibrations and acoustic noise. So it becomes challenging to produce sufficient flux at lower frequencies/ voltages (Richard et al., 2006; Ying-Yu-Tzou and Hau-Jean, 1997). A new control structure for digital realization of induction motor control has been developed based on space vector PWM VSI control through FPGA. Figure 2 shows the rectifier unit to convert single phase ac into dc which is fed to the IGBT inverter. The Xilinx compatible FPGA is used to control the IGBT gate driver circuit, for further implementing the volt per hertz speed control techniques for induction motor. Induction motor is most commonly used machine with its flexibility in terms of operation. IGBT as inverter has been chosen because it comprises fast switching characteristics of MOSFET and lower conduction loss of power BJT's. The principal function of FPGA is to maintain the output timing of the inverted waves by controlling the IGBT gate driver circuit. FPGA is generating the control pulses to keep the three phases 120^0 out of phase sine waves on which AC Induction motor thrives. A 600 V rating has been chosen for designing a three phase inverter which is operating from 200 - 230 VAC. H.V.I.C. technology requires integration of analog control circuits and high voltage level shifting devices together with the capability of the analog circuits ope-rating at high voltage DC bus. The steady-state RMS value of the per-phase inverter output current is about 5 A when the inverter operates with a maximum motor overload at a switching frequency of 27.6 MHz. To account for overload current transient conditions, the current rating of the switching device is set up to 1.5 times the value of the steady-state current. Thus overload rating is expected up to 7.5 A.

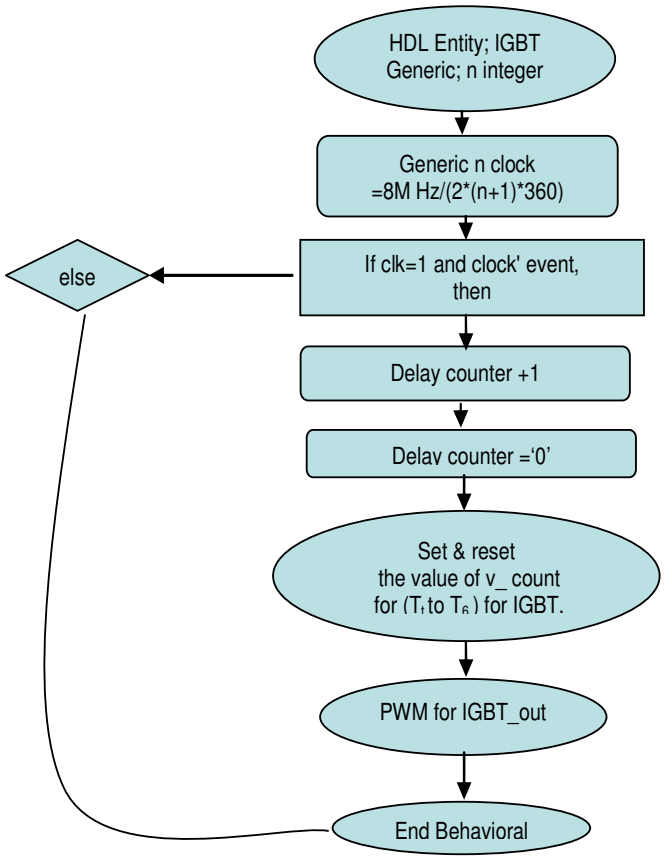

Figure 1. Flow Chart of coding.

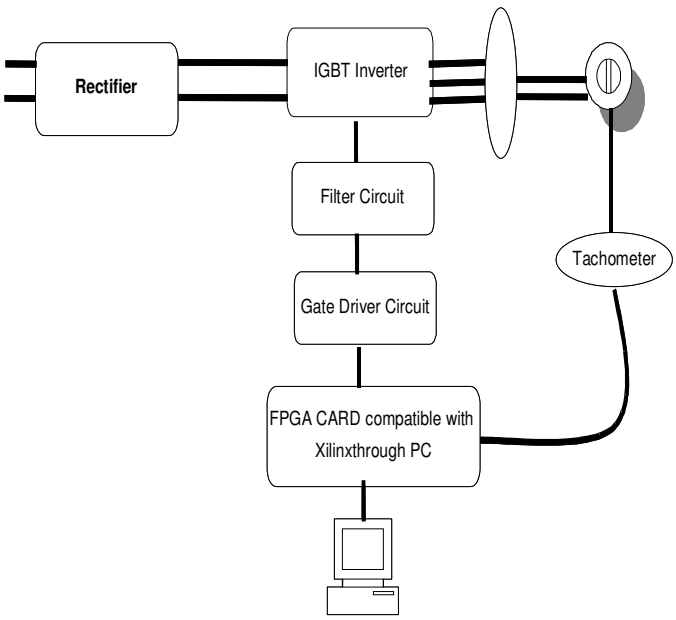

Figure 2. Block Diagram of experimental Setup for VSI controller through FPGA.

Table 1. Eight possible combinations of switching states.

R	Y	B	V_{RN}	V_{YN}	V_{BN}	V_{RY}	V_{YB}	V_{BR}	M	Ang.
0	0	0	0	0	0	0	0	0	0	0
0	0	1	-1/3	-1/3	⅔	0	-1	1	1	-120^0
0	1	0	-1/3	2/3	-1/3	-1	1	0	1	120^0
0	1	1	-⅔	1/3	1/3	-1	0	1	1	180
1	0	0	2/3	-1/3	-1/3	1	0	-1	1	0
1	0	1	1/3	-2/3	1/3	1	-1	0	1	-60^0
1	1	0	1/3	1/3	-2/3	0	1	-1	1	60^0
1	1	1	0	0	0	0	0	0	0	0

R, Y, B = Red, Yellow, Blue phases, V_{RN}, V_{YN}, V_{BN} = Line to neutral voltages, V_{RY}, V_{YB}, V_{BR} = Phase to Phase voltages, M = Magnitude, Ang. = Angle.

Table 2. Comparative table of different fpga.

Device	xc4003A	xc4010	xc2s50
Logic Cells	3,000	10,000	50,000
Total CLBs	100	400	384
Max. Available IOB	80	160	176
Distributed RAM Bits	3,200	12,800	24,576

Max. = maximum, IOBs = Input/Output Blocks, CLB = Configurable Logic Blocks; RAM = Random Access Memory.

Implementation of controlling algorithm

There are eight possible combinations of switching states which derived output line-to-line and phase voltages in terms of DC supply voltage V_{dc} according to equation no 1 to 3 and Table 1. Six of them lead to non-zero phase voltages and two interchangeable states lead to zero phase voltages.

Voltage across line –neutral

$$\left.\begin{aligned} V_{Rn} &= (V_R - V_n) = (V_{RY} - V_{BR})/3 \\ V_{Yn} &= (V_Y - V_n) = (V_{RY} - V_{BY})/3 \\ V_{Bn} &= (V_B - V_n) = (V_{BY} - V_{BR})/3 \end{aligned}\right\} \quad (1)$$

Voltage across line-line

$$\begin{bmatrix} V_{RY} \\ V_{YB} \\ V_{BR} \end{bmatrix} = (V_{dc}) \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} R \\ Y \\ B \end{bmatrix} \text{--} \quad (2)$$

$$\left.\begin{aligned} V_{RY} &= V_{Rdc} - V_{Ydc} \\ V_{YB} &= V_{Ydc} - V_{Bdc} \\ V_{BR} &= V_{Bdc} - V_{Rdc} \end{aligned}\right\} \text{-} \quad (3)$$

This intelligent controller comprise of software, power circuit and SVPWM in absolute unison. The floating point math algorithm succeeded in optimum designing of FPGA in combination of hardware and software. This high level integration on FPGA makes easier since it comprises 50,000 gates, a perimeter of input/output blocks (IOBs), a core array of configurable logic blocks (CLBs) and resources of interconnections.

Table 2 shows selection consideration of device no. xc2s50 for its superiority in specifications. More no. of gates/RAM size/ will give more features to be embedded hence this device has been chosen. Our studies have been performed on device xc2s50.

RESULTS

FPGA has endowed an attractive alternative in final product when total demand is restricted to few units because of high cost associated to ASIC fabrication. The hexagon shown in Figure 3 is 360^0 cycle with upper IGBT triggering through SVPWM in 60^0 interval of time.

This proposed operation is verified using HDL on Xilinx xc2x50 Spartan-II FPGA and the post layout timing results of the implementation are shown in Figure4. SVPWM is tested with the help of ModelSim5.4a with a frequency of f = 27.6 MHz are presented in timing simulation results the time period of start and end of the cycle is 87092300 ps and 87128477 ps respectively. It can seen that the switching sequence is changing for all six IGBTs after an equal interval of time. The switching pattern so generated has been varied to test the variation in speed of drive. The switching frequencies 27.6, 29.3,

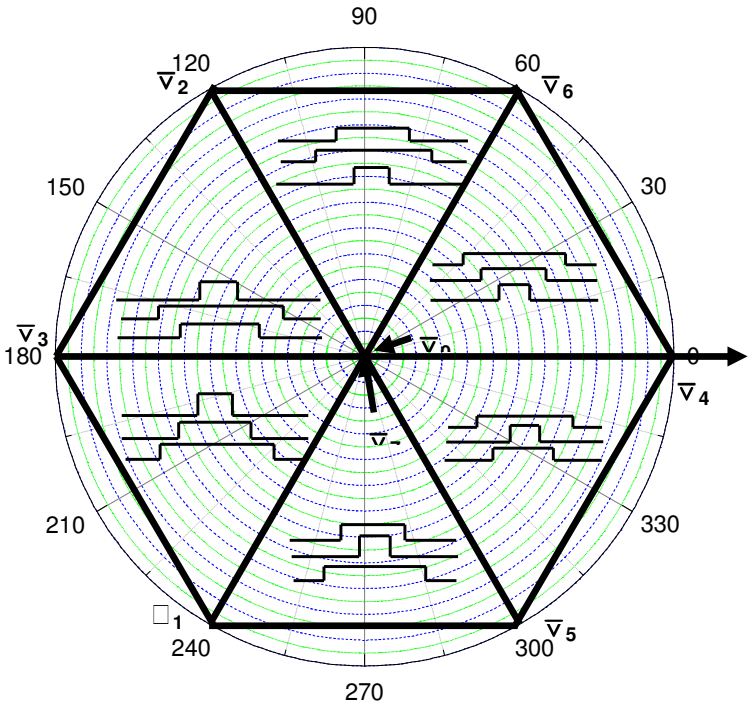

Figure 3. Hexagon of SVPWM, pattern.

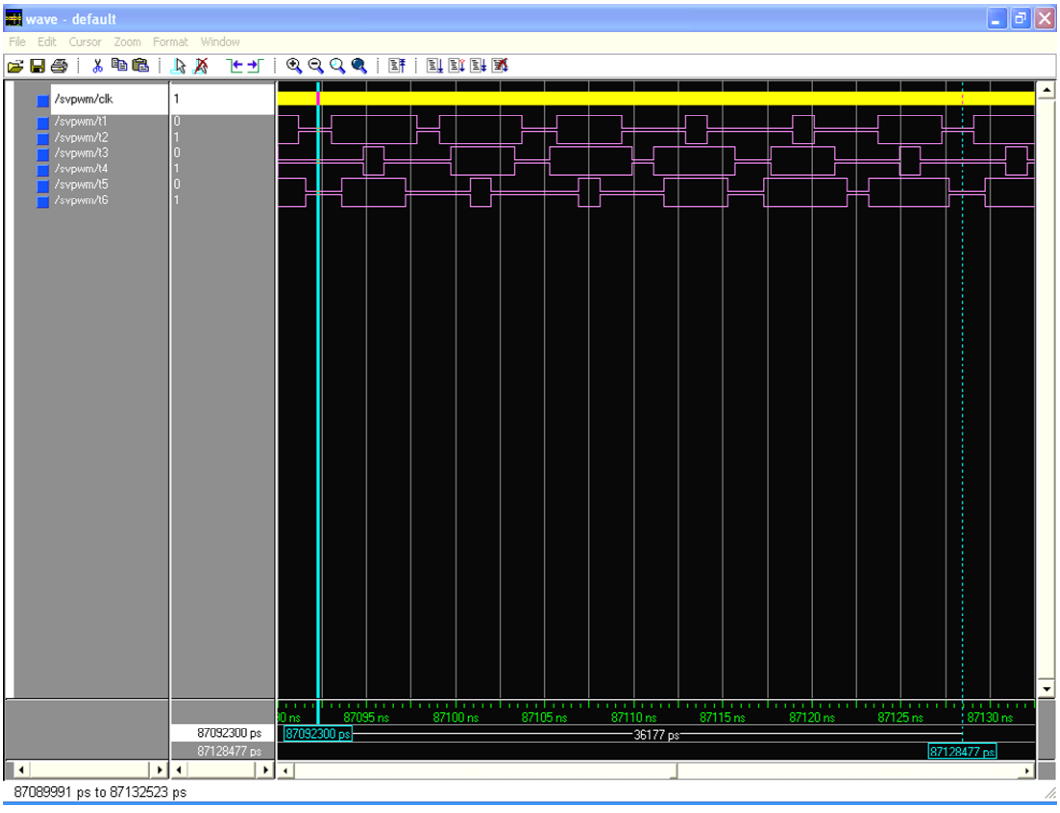

Figure 4. Timing Simulation of SVPWM (Space vector pulse width modulation).

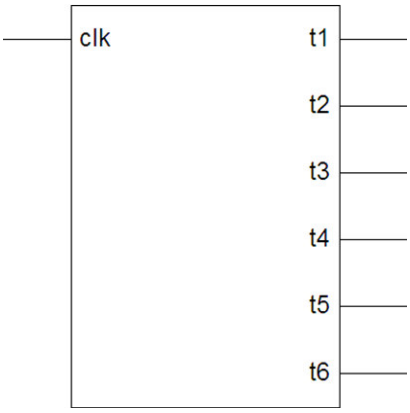

Figure 5. Integrated Circuit Structure of Xilinx program in FPGA.

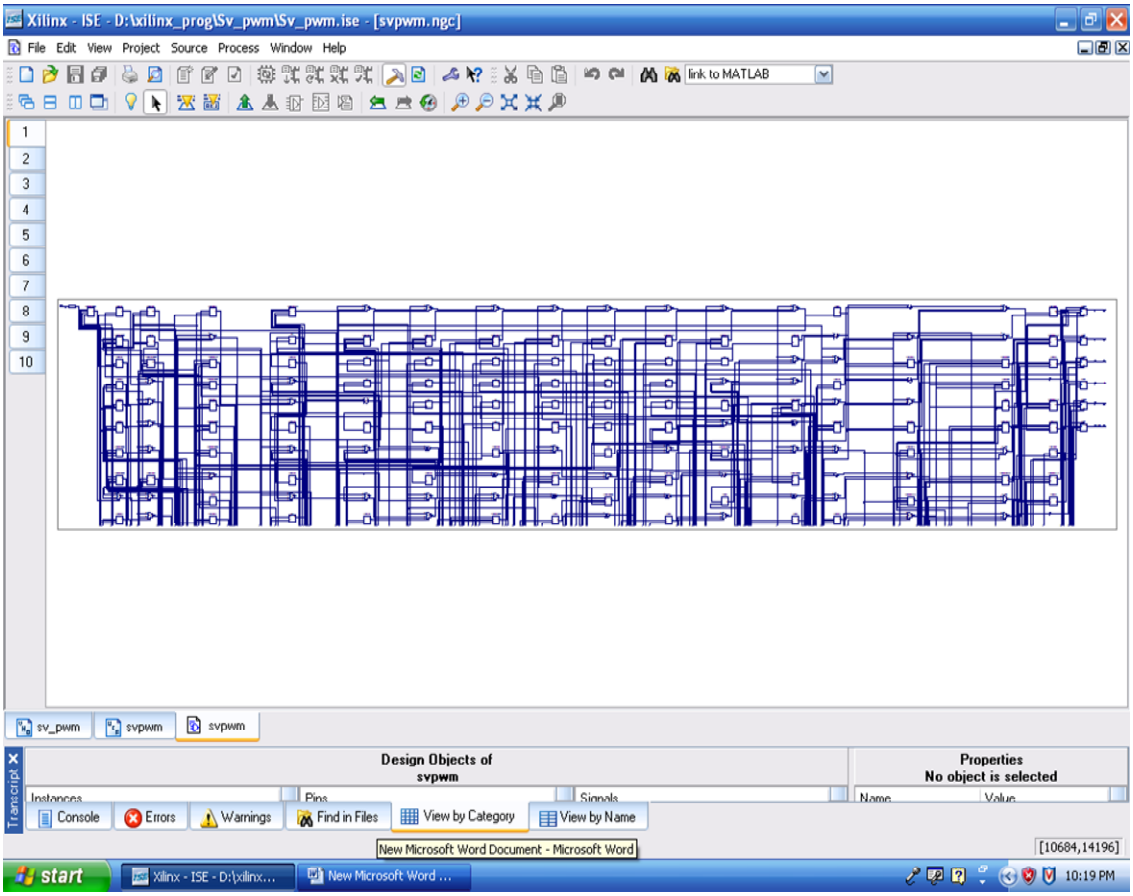

Figure 6. Schematic of SVPWM generators.

30.4, 26.2 and 25 MHz were set and a variation of 1267 to 1443 RPM was observed. The on field speed variation with the change in program application has also been proved with this test.

IC structure and Schematic of SVPWM generator of coding are shown in Figures 5 and 6 respectively. t_1 to t_6 shows the output from FPGA connected at gate driver circuitry of six IGBTs of inverter. Schematic presents the

Table 3. Comparative table of different fpga.

Logic utilization	Utilization
Number of Slice Flip Flops	23%
Number of 4 input LUTs	35%
Number of occupied Slices	74%
Number of Slices containing only related logic	100%
Total Number 4 input LUTs	70%
Number of bonded IOBs	12%
Number of GCLKs	75%
Number of GCLKIOBs	25%

occupation inside the FPGA after programming. The results articulate the algorithm perfectly. 70% 4-LUTs, 23% flip-flops slices and 12% bonded IOBs were utilized as shown in Table 3.

The proposed scheme has achieved good voltage regulation against load variations. Simulation results have proven the design principles and theoretical analysis.

Conclusion

The resulting tile structure indicates the optimal utilization of tile structure with presumption that the electronic structure would be a complex and bulky in circuitry. Also from Table 3 supports the above mentioned conclusion. The ease of reprogramming has facilitated the use to mould the structure values as per the suitability. A high variation in frequency has been observed. .

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