

Full Length Research Paper

Performance evaluation of multirate filters for digital down converters

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For achieving maximum signal transfer without any noise in all available communication systems, the frequency of the processor is synchronized with the sampling rate of the signal. The use of multirate filtering allows designers to achieve this. In this paper, the multirate filters with and without compensation have been implemented very effectively using FPGA (field programmable gate arrays). Also, comparison of FIR (finite impulse response) filters and differential delay farrow filters has been done for different sampling frequencies. The proposed filter structures have wide applications in the designing of sample rate converters, analog to digital converter, decimators and interpolators. It can be concluded from the design results that the proposed structures can be used efficiently in the designing of any communication system.

Key words: Multirate filters, compensation, DDC (digital down converter), WiMax (worldwide interoperability for microwave access), FPGA (field programmable gate arrays).

INTRODUCTION

Multirate systems are used extensively in all areas of digital signal processing (DSP). Their function is to alter the rate of the discrete-time signals, by adding or deleting a portion of the signal samples. They are essential in various standard signal processing techniques such as signal analysis, denoising, compression and so forth. During the last decade, however, they have increasingly found applications in new and emerging areas of signal processing, as well as in several neighboring disciplines such as digital communications.

The cascaded integrator comb (CIC) filter is a digital filter which is employed for multiplier-less realization of filters. This type of filter has extensive applications in low-cost implementation of interpolators and decimators. However, there are some drawbacks like pass-band

droop in this filter, but they can be eliminated using compensation techniques.

The farrow filters is another class of digital filters which are used extensively in arbitrary sample rate conversions and fractionally delaying the samples. They have polyphase structure and are very efficient for digital filtering. Field-programmable gate array (FPGA) has become an extremely cost-effective means of off-loading computationally intensive digital signal processing algorithms to improve overall system performance.

In this paper, CIC filter with and without compensation technique are implemented on FPGA. Also the farrow filters are implemented for fractional delay and arbitrary change in sample rate conversion. Both of these filters gives a better performance than the common filter structures in terms of speed of operation, cost, and power consumption in real-time. These filters are implemented in Altera Stratix-II-EP2S15F484C3 FPGA and simulated with the help of Quartus II v9.1sp2. These filters can work in real time.

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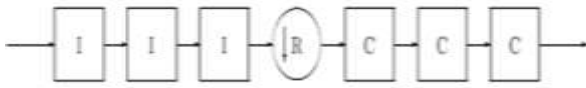


Figure 1. Three stage decimating CIC filter.

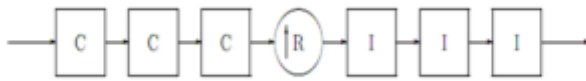


Figure 2. Three stage interpolating CIC filter.

Cascaded integrator comb (CIC) filters

The cascaded integrator-comb (CIC) filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters. CIC filters achieve sampling rate decrease (decimation) and sampling rate increase (interpolation) without using multipliers. A CIC filter consists of an equal number of stages of ideal integrator and comb filters. Its frequency response may be tuned by selecting the appropriate number of cascaded integrator and comb filter pairs. The highly symmetric structure of a CIC filter allows efficient implementation in hardware. However, the disadvantage of a CIC filter is that its pass band is not flat, which is undesirable in many applications. Fortunately, this problem can be alleviated by a compensation filter. The CIC filter can also be implemented very efficiently in hardware due to its symmetric structure.

A CIC decimator would have N cascaded integrator stages clocked at fs, followed by a rate change by a factor R, followed by N cascaded comb stages running at fs/R. A CIC interpolator would be N cascaded comb stages running at fs/R, followed by a zero-stuffer, followed by N cascaded integrator stages running at fs. This is shown in Figures 1 and 2.

The transfer function of the CIC filter in z-domain is given in equation (1).

$$H(z) = \left(\frac{1 - z^{-k}}{1 - z^{-1}} \right)^L \tag{1}$$

In Equation (1), K is the oversampling ratio and L is the order of the filter.

The numerator $(1 - z^{-k})^L$ represents the transfer function of a differentiator and the denominator $(1/(1 - z^{-1})^L)$

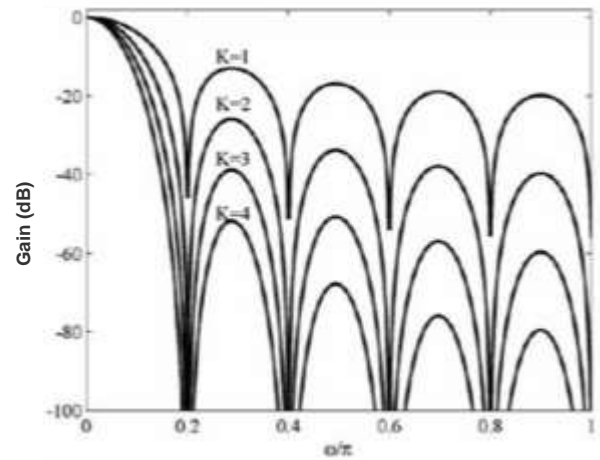


Figure 3. CIC filter gain responses: single-stage K = 1, two-stage K = 2, three-stage K = 3 and four-stage K = 4.

indicates the transfer function of an integrator (Hogenauer, 1981).

A very poor magnitude characteristic of the comb filter is improved by cascading several identical comb filters. The transfer function H(z) of the multistage comb filter composed of K identical single-stage comb filters is given by

$$H(z) = \left(\frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}} \right)^K \tag{2}$$

Figure 3 shows how the multistage realization improves the selectivity and the stop-band attenuation of the overall filter: the selectivity and the stop-band attenuation are augmented with the increase of the number of comb filter sections (Dolecek and Mitra, 2005). The filter has multiple nulls with multiplicity equal to the number of the sections (K). Consequently, the stop-band attenuation in the null intervals is very high. Figure 4 illustrates a monotonic decrease of the magnitude response in the pass-band, called the pass-band droop (Ljiljana, 2009).

CIC filters in decimation and interpolation

The CIC filters are utilized in multirate systems for constructing efficient decimators and interpolators. The comb filter ability to perform filtering without multiplications is very attractive to be applied to high rate signals. Moreover, CIC filters are convenient for large conversion factors since the low pass bandwidth is very small. In multistage decimators with a large conversion

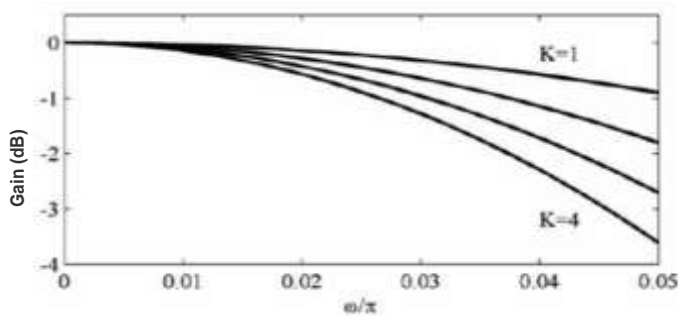


Figure 4. CIC Filter Gain Response: Pass-band droop for Figure 3.

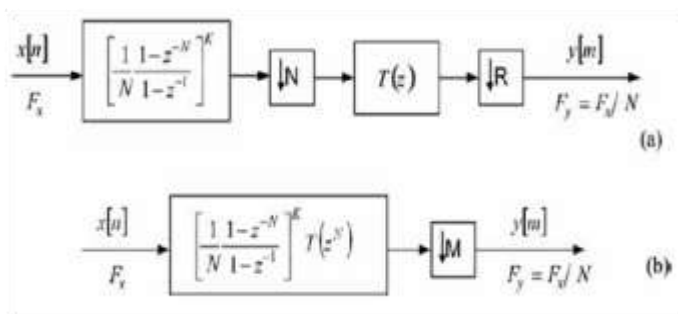


Figure 5. Two-stage decimator composed of a CIC filter and an FIR filter: (a) Cascade implementation. (b) Single-stage equivalent.

factor, the comb filter is the best solution for the first decimation stage, whereas in interpolators, the comb filter is convenient for the last interpolation stage (Hogenauer, 1981). The multirate application of comb filters has been proposed first by Hogenauer, and since that time, the so-called Hogenauer filters have attracted many researchers and practicing engineers.

Compensation of CIC filters

A CIC filter can be used as a first stage in decimation when the overall conversion ratio M is factorable as

$$M = N \times R \tag{3}$$

The overall factor-of- M sampling rate conversion system can be implemented by cascading a factor-of- N CIC decimator and a factor-of- R FIR decimator (Abu-Al-Saud and Stuber, 2003) as shown in Figure 5(a). The corresponding single-stage equivalent is given in Figure 5(b). When constructing an interpolator with a conversion factor L factorable as

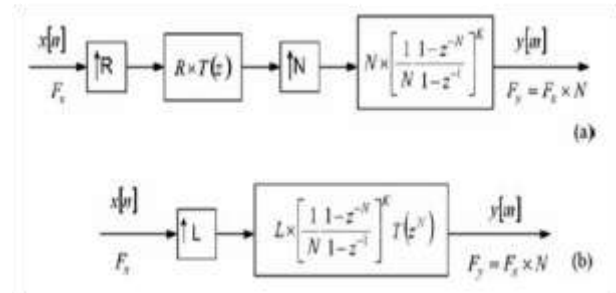


Figure 6. Two-stage interpolator composed of an FIR filter in the first stage, and the CIC filter in the second stage: (a) Cascade implementation. (b) Single-stage equivalent.

$$L = R \times N \tag{4}$$

It might be beneficial to implement the second (last) stage as a CIC interpolator (Ljiljana, 2009). The first stage is usually implemented as an FIR filter. Figure 6(a) depicts the two-stage interpolator consisting of the cascade of a factor-of- R FIR interpolator and a factor-of- N CIC interpolator. The corresponding single-stage equivalent is shown in Figure 6(b).

In the two-stage solutions of Figures 5 and 6, the role of CIC decimator (interpolator) is to convert the sampling rate by the large conversion factor N , whereas the FIR filter $T(z)$ provides the desired transition band of the overall decimator (interpolator) and compensates the pass-band characteristic of the CIC filter.

Filter $T(z^N)$ ensures the desired transition band, compensates the pass-band droop of the comb filter of the first stage. The CIC filter $H(z)$ has its two nulls just in the undesired pass-bands of the periodic filter $T(z^N)$ that ensure the requested stop-band attenuation of the target two-stage decimator (Jiang and Junior, 1997). Finally, we compute the frequency response of the overall two-stage decimation filter (Ljiljana, 2009; Crochiere and Rabiner, 1983). Figure 7 shows the gain response of CIC and FIR filter and figure 8 shows the Gain responses of the two-stage decimator implemented as a factor-of-5 decimator and a factor-of-two FIR decimator

$$H_1(z) = H(z) \cdot T(z^N) \tag{5}$$

Filters with non integer decimation factor: Farrow filters

When the decimation factor $1/R$ or the interpolation factor R is an integral value, then the conversion of sampling rate can be performed conveniently with the aid of fixed digital filters (Farrow, 1998). In case of a scenario where

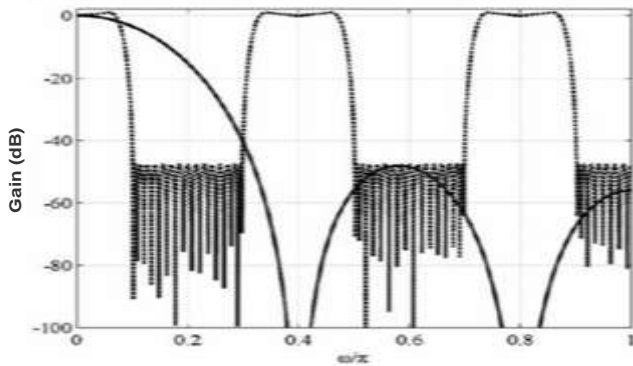


Figure 7. Gain responses of the CIC filter $H(z)$ (solid line), and that of periodic FIR filter $T(z^5)$ (dashed line).

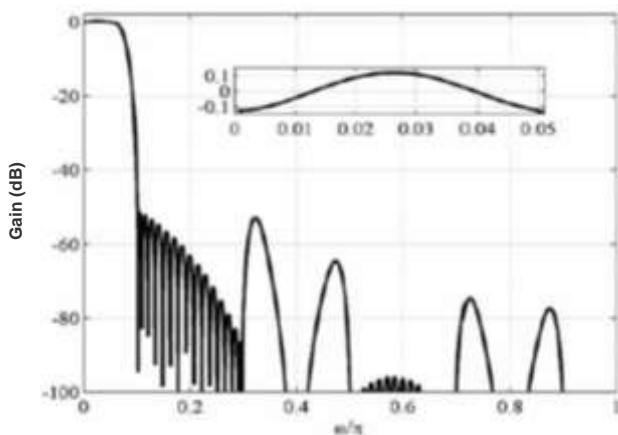


Figure 8. Gain responses of the two-stage decimator implemented as a factor-of-5 decimator and a factor-of-two FIR decimator.

the factors are irrational, it will be impossible to use fixed digital filters directly. Moreover, if R is considered as the ratio of two relatively large prime integers, then, in the case of the conventional polyphase implementation, it is quiet essential that the orders of the required filter become very large (Oh et al., 1999). In nutshell, it means that a large number of coefficients need to be stored in coefficient memory. In sampling rate conversion by non-integer factor, it is required to determine the values between existing samples. In this case, it is very convenient to use interpolation filters. Among them, polynomial-based filters are generally assumed to provide an efficient implementation form directly in digital domain. Such filters witness an effective implementation through Farrow structure or its higher version (Farrow,

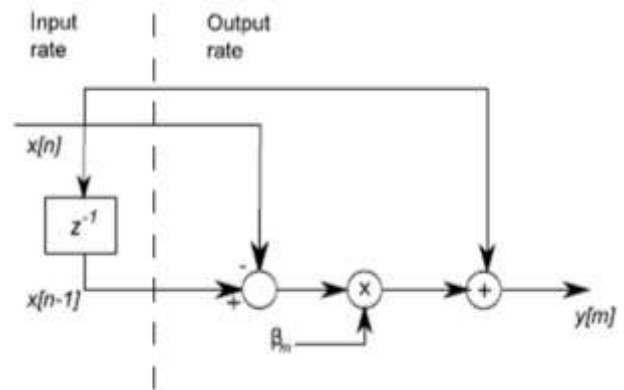


Figure 9. Multirate farrow filter.

1998; Hentschel and Fettweis, 2000). The main advantage of the Farrow structure is based on the presence of fixed finite-impulse response (FIR) filters as one of its ingredients. Thus, there is only one changeable parameter being the so-called fractional interval μ . Besides this, the control of μ is easier during the operation than in the corresponding coefficient memory implementations, and the concept of arithmetic preciseness; not the memory size limits the resolution of μ . These characteristics of the Farrow structure make it a very attractive structure to be implemented using a VLSI circuit or a signal processor (Vesma, 1999; Fettweis and Hentschel, 2000).

Consider the diagram shown in Figure 9. The dashed line separates the filter into a section running at the input signal's sampling-rate and a section running at the output sampling-rate. Note that the output is re-labeled to be $y[m]$ rather than $y[n]$. This is due to different input and output rates. Notably, the fractional delay denoted as βm will now change at every instant an output sample occurs.

Now consider a case where the sampling rate is increased by a factor of 2. Since for every input there are two outputs, the value held in the delay register will be used twice. The first time an input is used, βm will take on the value 0.5 and the output will be computed as

$$y[m] = 0.5(x[n-1] - x[n]) + x[n] = 0.5x[n-1] + 0.5x[n] \quad (6)$$

Before the input sample changes, one more output sample will be computed. βm will take the value 0 and the output will simply be

$$y[m+1] = x[n] \quad (7)$$

Subsequently, the input sample will change; βm will be

once again set to 0.5 and so forth. In summary, when increasing the sampling rate by a factor of two, β_m will cycle between the values $\{0.5, 0\}$ twice as fast as the input, producing an output each time it changes.

In the general case, it is simply a matter of determining which values β must take. The formula is simply

$$\beta_m = \left(\frac{mf_s}{f_s} \right) \bmod 1 \quad (8)$$

Where f_s is the input sampling rate and f'_s is the output sampling rate.

In order to perform a non integer SRC (sample rate conversion), Farrow structure or its modifications directly can be used. However, in many cases, it becomes more efficient to use cascaded structures engineered by the modification of the Farrow structure and fixed FIR, or multistage FIR filter (Babic et al., 2001, 2002, 2005; Meyer and Bease, 2007). The main advantage of using the cascaded structures instead of the direct modification of the Farrow structure lies in the fact that in case of joint optimization of the two building blocks the computational complexity to generate practically the same filtering performance is dramatically reduced. This is because of the following reasons. First, the implementation of a fixed linear phase FIR interpolator is not very costly, compared to the Farrow structure. Second, most importantly, the requirements for implementing the modification of the Farrow structure become significantly milder. This is mainly because the FIR filter takes care of pass-band and stop-band shaping, where the Farrow-based structure should only take care of attenuating images of FIR filter (Vesma and Saramaki, 2007).

RESULTS AND DISCUSSION

This section illustrates the properties of the proposed filters by means of design examples.

Comparison of CIC filters with and without compensation

The specifications for DDC for WiMax are as follows:

- Input Sampling Frequency: 91.392 MHz
- Output sampling frequency: 11.424 MHz
- Pass-band edge: 4.75 MHz
- Pass-band ripple: 0.14 dB
- Stop-band attenuation: 92 dB

Simulation results of CIC filter

Simulation results of CIC filter are shown in Figures 10

and 11. Figure 10 show the magnitude response of DDC for WiMax using CIC filters and Figure 11 show Modelsim simulation of DDC for WiMax using CIC filters.

Simulation results of CIC filter with compensation

Simulation results of CIC filter with compensation are shown in Figures 12a, 12b and 13. From the simulation results shown in Figures 12 and 13 and implementation results shown in Table 1, it can be concluded that the CIC filter are efficient for low-cost implementations. Due to absence of multipliers, they also have faster response. But the pass-band droop present in CIC filters restricts the scope of applications. With compensation technique, the response of CIC filter in pass-band is improved, but at the cost of extra hardware.

Comparison of FIR and Farrow sample rate conversions

Consider a design example to change the sampling rate by a factor of 1.536 (192/125). The design to change the sample rate by an arbitrary factor is considered. The results obtained for the simulations are shown in Figures 14, 15 and 16.

Both of these filters are also implemented efficiently in Altera's Stratix II FPGA family with device number EP2S15F484C3.

From Figure 14 and Table 2, it is clear that the Farrow structure is better than the normal FIR filter. The efficiency of Farrow filters is more as compared to other one as the amount of logic utilization required for the coefficients of Farrow filter is much less as compared to FIR filter. Secondly, the response of the Farrow filter for same SRC is much faster as compared to FIR SRC.

All these sum-up to prove that the Farrow filters are more efficient in implementation as compared to the FIR structure.

Conclusion

By the use of Application Specific Integrated Circuits, in device designing of embedded systems and in signal processing results in improvement of the characteristics and specification of the devices. But, with the change in specifications requires redesigning of that particular system, which in turn increases the cost. With the advancement in FPGA Technology, the devices with more speed and configuration are available and moreover the specifications can also be altered without redesigning the whole system, thus reducing the cost to

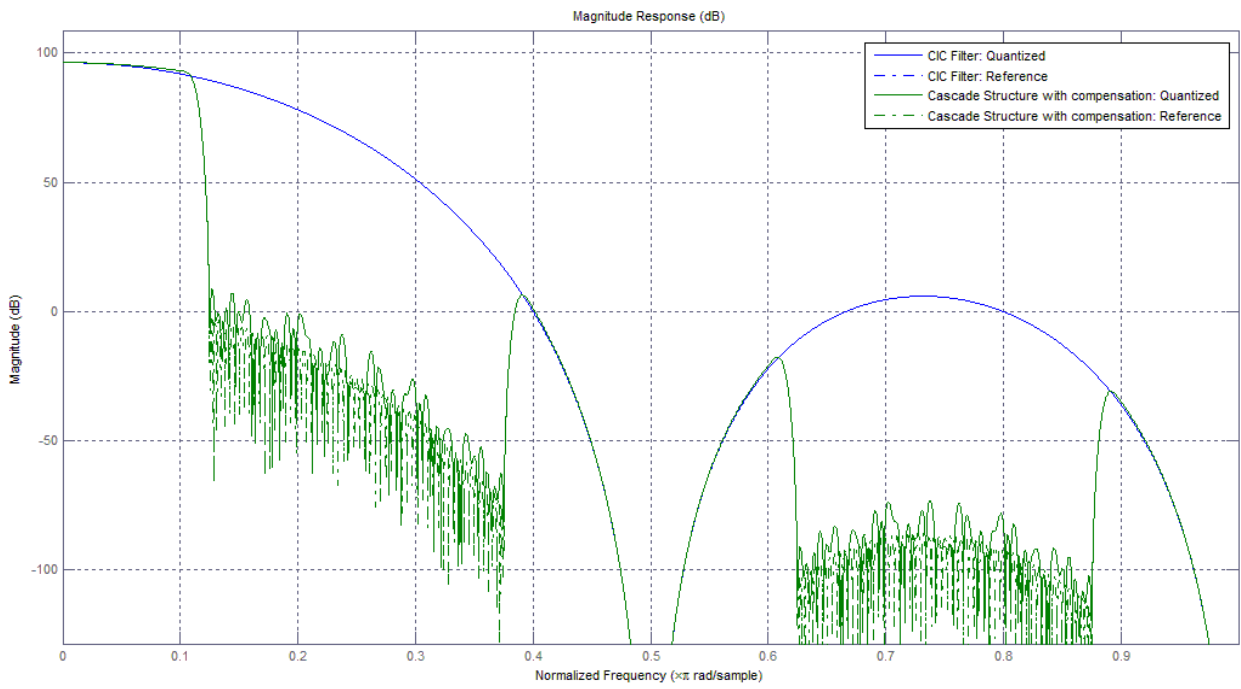


Figure 12a. Magnitude response of DDC for WiMax using CIC filters using compensation.

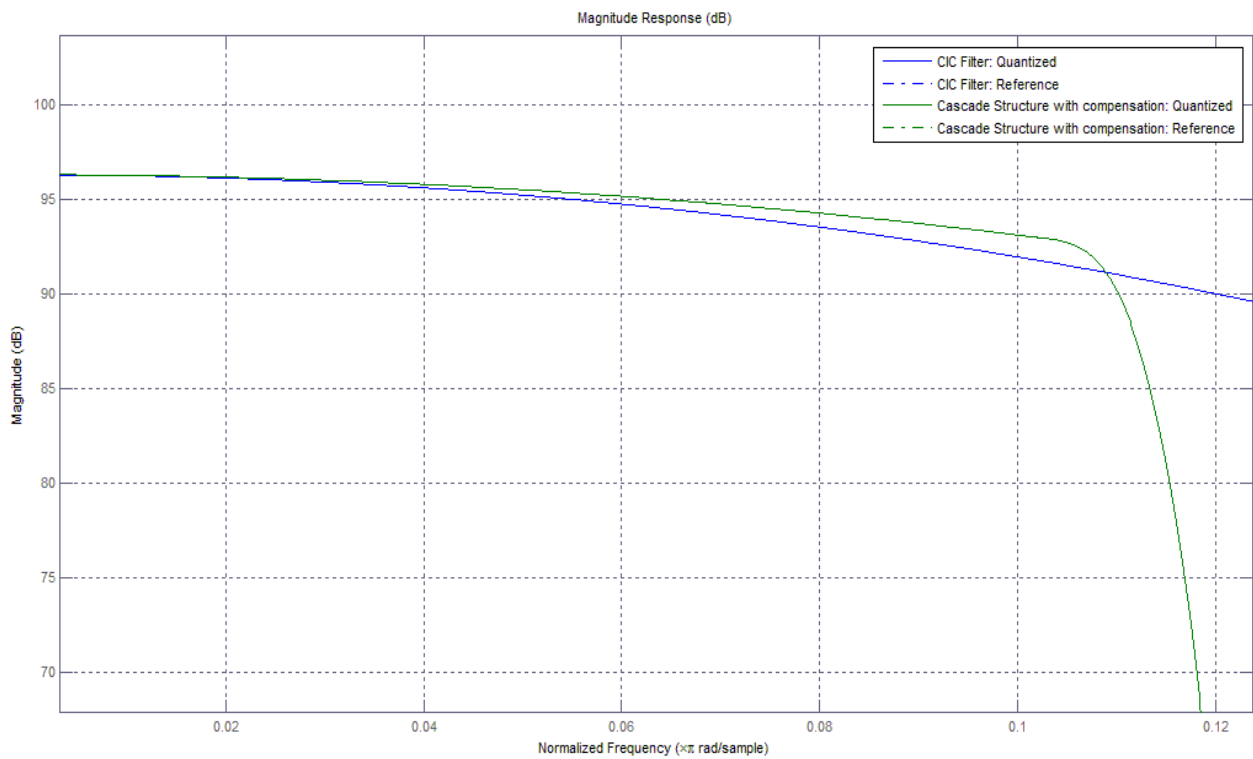


Figure 12b. Magnitude response of ddc for WiMax using CIC filters with compensation: expanded view.

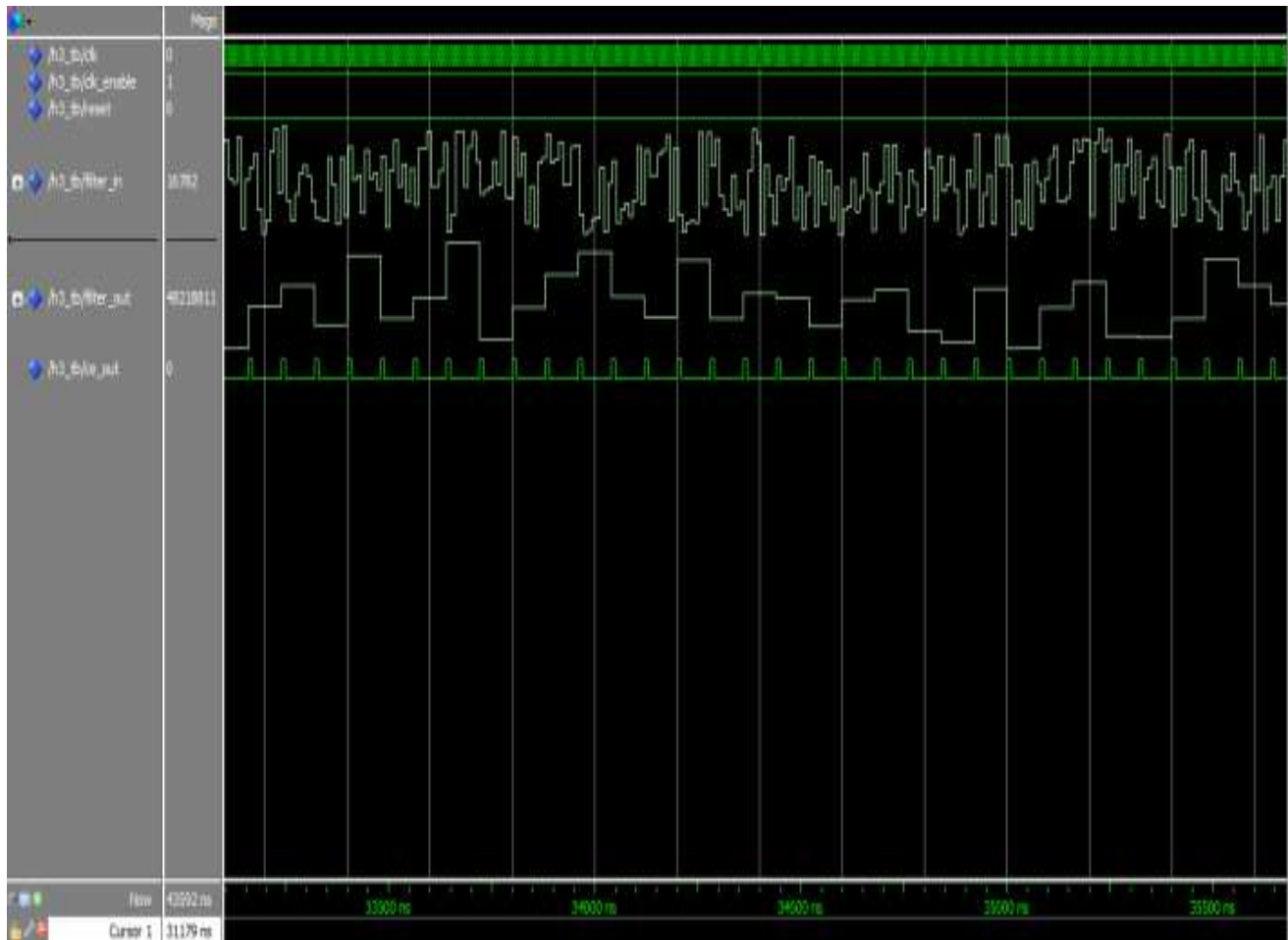


Figure 13. Modelsim simulation of DDC for WiMax using CIC filters with compensation.

Table 1. Comparison of implementation cost and speed analysis of CIC filter and its cascaded structure with compensation.

| Property | CIC filter | Cascaded CIC filter with compensation |
|-------------------------------------|------------|---------------------------------------|
| Logic utilization | 29% | 63% |
| t_{su} (Worst Case Set Up Time) | 7.425 ns | 6.654 ns |
| t_{cq} (Worst Case CLK to Q Time) | 7.379 ns | 6.619 ns |
| Clock frequency | 203.54 MHz | 21.91 MHz |

minimum and optimum use can be done with the available resources.

In this paper, CIC filter and cascaded CIC filter for compensation is implemented in Altera's Stratix II FPGA

for the specifications of Digital Down Converter of WiMax. Though the CIC filters have upper hand on the basis of cost of implementation and speed, but the response of compensated CIC filter proves to be more reliable.

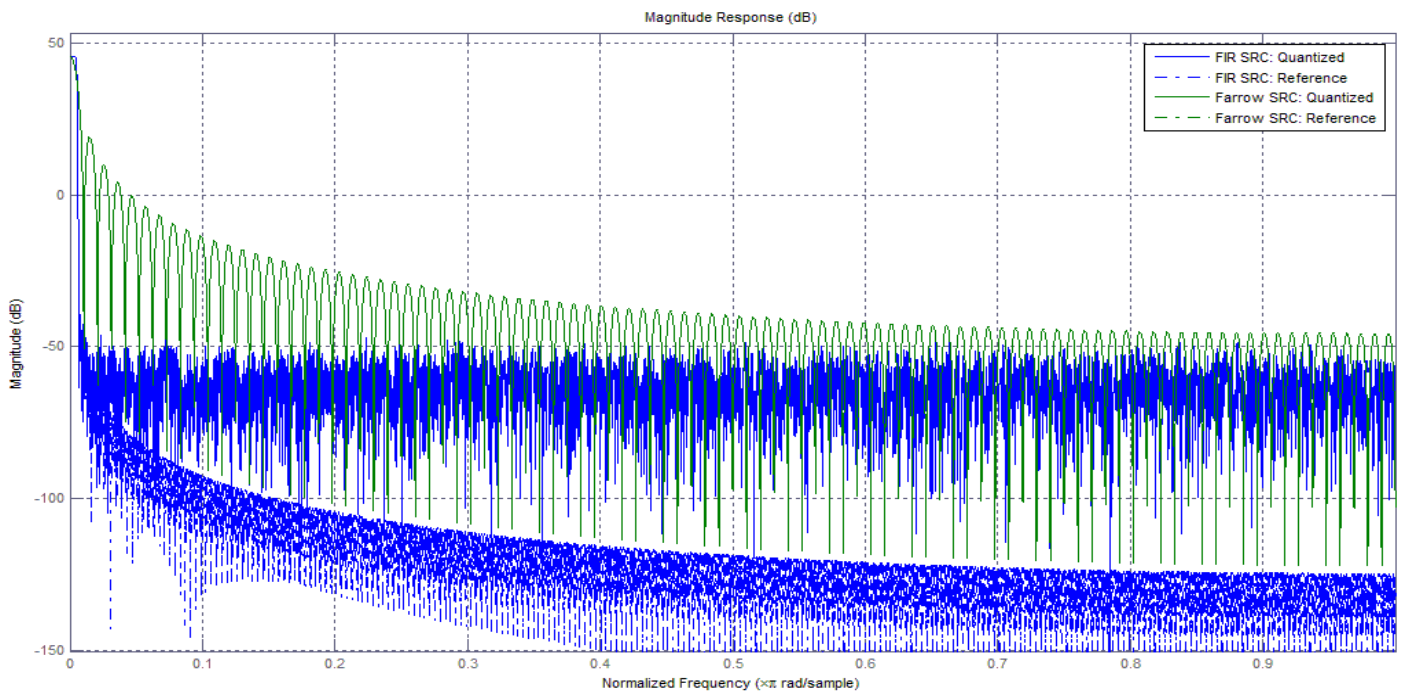


Figure 14. Response of FIR SRC(blue) and Farrow SRC(green) for the factor of 1.536 change in sample rates.

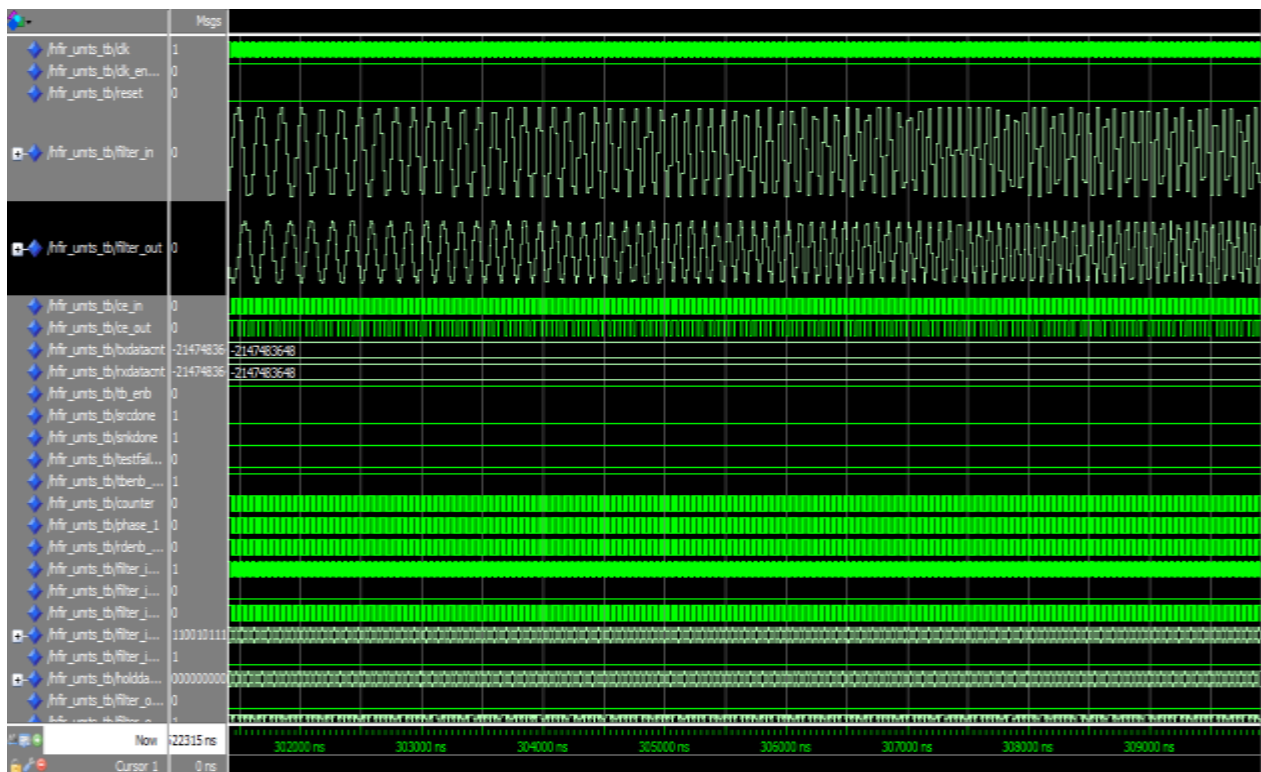


Figure 15. Modelsim simulation of FIR SRC.

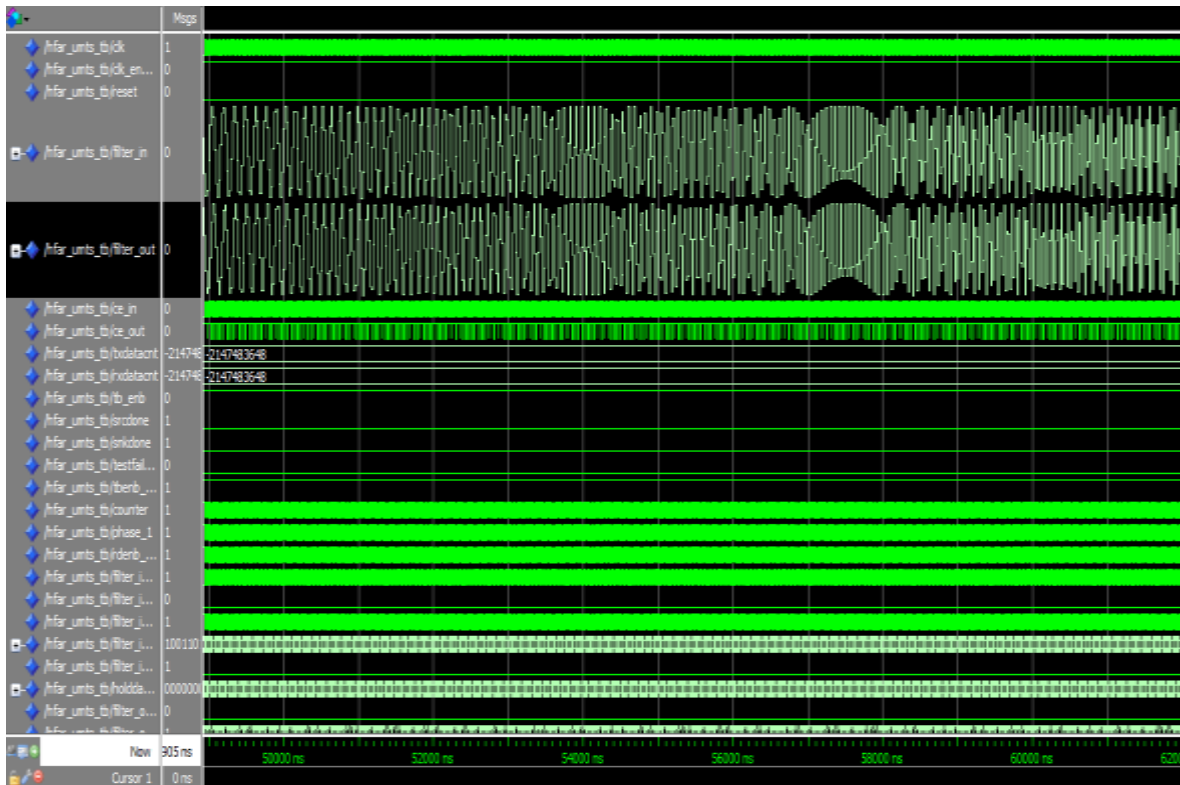


Figure 16. Modelsim simulation of Farow SRC.

Table 2. Comparison of implementation cost and speed analysis of FARROW and FIR SRC.

| Property | Farrow SRC | Fir SRC |
|-------------------------------------|------------|-----------|
| Logic Utilization | < 1% | 40% |
| t_{su} (Worst Case Set Up Time) | 4.793 ns | 7.473 ns |
| t_{cq} (Worst Case CLK to Q Time) | 7.233 ns | 6.944 ns |
| Clock frequency | 306.18 MHz | 49.66 MHz |

Apart from CIC filters, Farrow filters are also implemented on FPGA for SRC. A comparison is shown for FIR SRC and Farrow SRC, which shows that the Farrow filters are more superior in implementation than FIR filters for Arbitrary SRC Design as the logic utilization and speed of the filter is improved.

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